COTS JOURNAL

Tech Focus: Rugged Displays

RUGGED ETHERNET BOARDS EMBRACE FABRIC ROLES

PLUS:

FPGAs Flex Their Computing Muscles

Test Schemes Improve MTBF Prediction

Volume 10 Number 06 June 2008 www.cotsjournalonline.com

An RTC Group Publication

DDC®
®Data Device Corporation

TOOLS OF INNOVATION

Ideal for
lab applications

DDC's Family of USB Interfaces...
Small, Lightweight, and Portable.

- MIL-STD-1553 and ARINC 429
- Graphical User Interface
- High Channel Count
- USB Powered

Ideal for
rugged/embedded
applications

www.ddc-web.com **Toll Free: 1-800-DDC-5757**

COTS JOURNAL

Features

June 2008 Volume 10 Number 6

Special Feature

Ethernet Switches for Military Apps

Tech Recon

The FPGA Computing Revolution

System Development

New Approaches to Military Test

Technology Focus

Rugged Displays

COTS (kots), *n.* **1.** Commercial off-the-shelf. Terminology popularized in 1994 within U.S. DoD by SECDEF Wm. Perry's "Perry Memo" that changed military industry purchasing and design guidelines, making Mil-Specs acceptable only by waiver. COTS is generally defined for technology, goods and services as: a) using commercial business practices and specifications, b) not developed under government funding, c) offered for sale to the general market, d) still must meet the program ORD. **2.** Commercial business practices include the accepted practice of customer-paid minor modification to standard COTS products to meet the customer's unique requirements.

——**Ant.** When applied to the procurement of electronics for the U.S. Military, COTS is a procurement philosophy and does not imply commercial, office environment or any other durability grade. *E.g., rad-hard components designed and offered for sale to the general market are COTS if they were developed by the company and not under government funding.*

Departments

Coming in July...
...See Page 64

Cover Story ..... Page 12

Ethernet-based IP technology is used in Raytheon's SSDS Mk 2 (Ship Self-Defense System) program, which can be found on ships such as the aircraft carrier USS Ronald Reagan (CVN 76). Raytheon uses Performance Technologies' Advanced Managed Platform IP-comms platform to provide an IP-based networking platform for the SSDS system. Shown here, flight deck crew aboard the Ronald Reagan direct a C-2A Greyhound onto a launch catapult.

U.S. Navy photo by Mass Communication Specialist 3rd Class Joe Painter

Innovation sets us apart

Avionics Databus Test, Simulation & Embedded Solutions

Lightweight, small, rugged, reliable, feature rich and cost-effective. These are only a few of the benefits of the new AB2000 series of Avionics BusBoxes® from Ballard Technology. They deliver outstanding avionics performance with multi-protocol and flexible expansion capabilities. Conductively cooled, the AB2000 is ideal for rugged avionics applications such as serving and recording data, converting protocols and providing federated control. Find out today how AB2000 innovation can work for you.

The AB2000 offers multi-protocols in a single, lightweight rugged format.

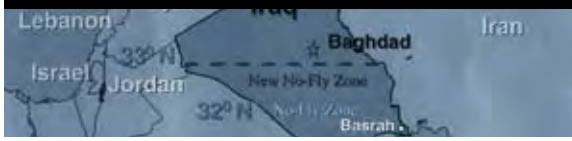
ARINC 429
MIL-STD-1553
Ethernet
RS232/422
Digital I/O
USB

Innovation for your success

For more information call 425.339.0281 or visit us at www.ballardtech.com

Ballard TECHNOLOGY

Publisher's Notebook



Budgets, Politicians and Carpetbaggers

Not to be disappointed during this season of politics, the U.S. Senate Armed Services Committee met in a secret session at the end of April and voted to support spending $542.5 billion along with a $70 billion kicker for Iraq and Afghanistan. I'm sure there was a security reason to having a secret session, and not a political reason with elections coming up at the end of the year. Now no one can question how any particular member has positioned themselves regarding the budget. Everyone can only blame the group. Both sides of the aisle apparently acknowledged that the $70 billion for the war is only a down payment to get the new President through the first few months in office without having to cope with that issue. SECDEF Gates estimates that at least another $100 billion will be needed to fund the war.

The current administration only asked for $605.7 billion for 2009 including the war. If I do my addition right, adding the Armed Services Committee number to Gates' expected $100 billion kicker, the total comes to a proposed $712.5 billion dollars for 2009. That's almost 18% more than requested. What happened to the universal outcry to reduce the government's budget and the deficit?

As per usual, the Senators shifted funds from one program to another. Now, I definitely think that we need to have congressional oversight to spending. To me that means controlling funds being spent because of mismanagement or because there is no rational justification for spending it. But I have a tough time with politicians saying to the DoD "you will spend more money on this program, or you will resurrect this program and fund it even if you don't want it." And then those same politicians accuse military leaders of having an aging military and not being as prepared or effective as they should be.

Most recently the House leadership—with limited or no additional House input—produced a war-spending bill for $162.5 billion dollars to cover war activities into the summer of 2009. The bill's conception—and the limits on what input different elements of the House of Representatives could provide—resulted in a bi-partisan defeat of the bill. Now everyone is pointing fingers at everyone else and trying to put their own political spin on what is happening with this issue. What we should really consider is an oversight committee for Congress. For that matter, I guess we could add a few other elements of government needing an independent non-congressional oversight committee.

Shifting to something more granular, let's talk about Directive 5000 series acquisition policies. The supposed outline for the military to develop, acquire and oversee its programs is getting another—repeat the word another a few dozen times—review and potential reform. The Pentagon pundits are saying that by fixing some of the steps that move a program too quickly forward without a thorough design review, cost plan and accurate performance schedule, its possible to drive down some of the astronomical program costs. This may come across as being very cynical—and I am—but it's clear to me that in a time of military operations, it is essential to ensure the troops get what they need for the operations as quickly as possible.

What the DoD doesn't need are carpetbaggers. And with today's sky-high program costs and associated profitability to major suppliers, someone needs to put things back on track. So what are the chances that this attempt will have any success? ZERO. Neither the Administration, Congress nor the Primes have any interest in fixing this. It's been going down hill for more than ten years and all these players have personal motives limiting their desire for things to change.

Defense Secretary Robert M. Gates and Navy Adm. Michael G. Mullen, chairman of the Joint Chiefs of Staff, testify before the Senate Armed Services Committee regarding the Defense Authorization Request for 2009 and continuing funding for Iraq and Afghanistan operations.

All that said, in spite of all the things that seem to be out of whack, embedded computing in the military will continue to grow. One of the largest growth areas will be in the ultra-small electronic systems for expendables, manpacks and autonomous systems.

Pete Yeatman, Publisher
COTS Journal

COTS JOURNAL

Publisher

PRESIDENT
John Reardon, johnr@rtcgroup.com

PUBLISHER
Pete Yeatman, mail@yeatmangroup.com

EDITORIAL DIRECTOR / Associate Publisher
Warren Andrews, warrena@rtcgroup.com

Editorial

EDITOR-IN-CHIEF
Jeff Child, jeffc@rtcgroup.com

CONTRIBUTING EDITOR
David Cotton, davidc@rtcgroup.com

MANAGING EDITOR
Marina Tringali, marinat@rtcgroup.com

COPY EDITOR
Rochelle Cohn

Art/Production

CREATIVE DIRECTOR
Jason Van Dorn, jasonv@rtcgroup.com

ART DIRECTOR
Kirsten Wyatt, kirstenw@rtcgroup.com

GRAPHIC DESIGNER
Christopher Saucier, chriss@rtcgroup.com

DIRECTOR OF WEB DEVELOPMENT
Marke Hallowell, markeh@rtcgroup.com

WEB DEVELOPER
James Wagner, jamesw@rtcgroup.com

INTERN
Andrew Fuller, andrewf@rtcgroup.com

Advertising

WESTERN REGIONAL ADVERTISING MANAGER
Stacy Gandre, stacyg@rtcgroup.com
(949) 226-2024

WESTERN REGIONAL ADVERTISING MANAGER
Lauren Hintze, laurenh@rtcgroup.com
(949) 226-2014

EASTERN REGIONAL ADVERTISING MANAGER
Nancy Vanderslice, nancyv@rtcgroup.com
(978) 443-2402

EASTERN REGIONAL ADVERTISING MANAGER
Todd Milroy, toddm@rtcgroup.com
(267) 247-5866

INSIDE SALES MANAGER
Carrie Bowers, carrieb@rtcgroup.com
(949) 226-2029

BILLING
Maggie McAuley, maggiem@rtcgroup.com
(949) 226-2024

COTS Journal

HOME OFFICE

The RTC Group, 905 Calle Amanecer, Suite 250, San Clemente, CA 92673
Phone: (949) 226-2000 Fax: (949) 226-2050, www.rtcgroup.com

EDITORIAL OFFICES

Warren Andrews, Editorial Director/Associate Publisher
39 Southport Cove, Bonita, FL 34134
Phone: (239) 992-4537 Fax: (239) 992-2396

Jeff Child, Editor-in-Chief
20A Northwest Blvd., PMB#137, Nashua, NH 03063
Phone: (603) 429-8301 Fax: (603) 424-8122

Published by THE RTC GROUP

Building a bigger future for MicroTCA

Because we know that overall system performance and reliability is crucial, we build product to ensure that your's comes out on top.

Our service to the aerospace and telecommunications markets has resulted in a quickly growing line of AdvancedTCA, MicroTCA, AMC, cPCIe, VXS, XMC and custom boards for processing, communication, storage, and platform interoperability.

At VadaTech we differentiate ourselves from other embedded computer manufacturing companies by incorporating our customers' vision into the product specification and development process; all the way through to deployment. Our partnership philosophy with our customers expands their engineering resources, increasing their value.

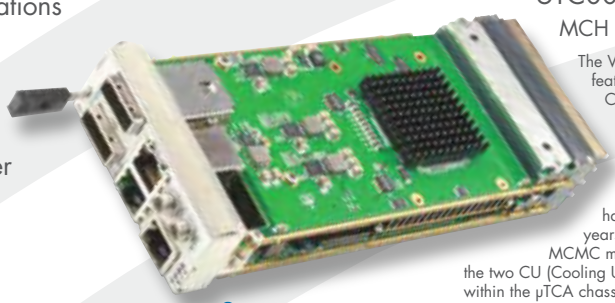
Overall design is only as good as it's weakest link, that is why we stop at nothing to ensure the best products for our clients.

VadaTech is a leader in:

- AdvancedTCA
- MicroTCA
- cPCIe
- XMC
- AMC
- VXS
- Custom Board-Level Technology

UTC001

MCH for MicroTCA Chassis



The VadaTech UTC001 is the most feature-rich MCH (MicroTCA Carrier Hub) for the µTCA chassis in the market. It's management software is based on VadaTech's robust Carrier Manager and Shelf Manager which have been deployed for many years with proven results. The MCMC manages the power modules, the two CU (Cooling Units) and the 12 AMCs within the µTCA chassis. It also interfaces to and manages the on-board fabric interfaces. The module is available with PCIe, SRIO, 10GbE, GbE and SAS fabric interfaces.

vadatech inc.

THE POWER OF VISION

WWW.VADATECH.COM

TEL 1.702.896.3337

GE Fanuc
Intelligent Platforms

This page isn't big enough to show all our switches.

With 43 Ethernet switches to choose from, you're sure to find what you need.

At GE Fanuc Intelligent Platforms, we have an extremely large portfolio of Ethernet switches, with a wide variety of form factors, media types, number of ports, management types and levels of ruggedness. Which greatly increases your chances of finding the switch you need.

You can choose from Ethernet switches in CompactPCI®, VME, PMC, VPX, VXS, custom form factors and rear transition modules. Your switch options include unmanaged, configuration managed and fully managed. You can have full control and monitoring, with local and remote access, provided by our OpenWare™ and FASTPATH™ management software. You have your choice of air cooled, conduction cooled and rugged air cooled switches—some of our switches are even available in five ruggedization levels.

Not only do we offer you maximum selection, but the switches themselves provide maximum flexibility, performance and density. Our firmware for fully managed switches supports IPv4/IPv6, Layer-2 and Layer-3 switching and routing at wire speed, plus support for Layer-3 protocols such as OSPF, RIP, VRRP, and MTSP. We have Gigabit Ethernet, 10Gb/s uplink ports for expansion, and the list goes on. In fact, this page can't hold it all, so visit our website at **www.gefanucembedded.com/switches** for all the details.

GE FANUC

The Inside Track

Curtiss-Wright to Supply Processor Modules for Future Combat Systems ICS

General Dynamics C4 Systems and Rockwell Collins have awarded an $8 million contract to Curtiss-Wright Controls to provide VPX-based General Processor Modules (GPM) for use in the Integrated Computer System (ICS) of the U.S. Army's Future Combat Systems (FCS) program. The Integrated Computer System combines a wide range of previously independent computing applications into a single, integrated, secure processing environment. ICS is a common computing environment for 13 of the 14 platforms in the FCS family of systems, which comprises a network of sensors, unmanned aerial platforms and manned and unmanned ground systems. Figure 1 shows the MULE, one of the unmanned FCS vehicles.

Figure 1

One of the FCS program's unmanned vehicle platforms, this version of the Multifunctional Utility/Logistics & Equipment Vehicle (MULE), called the MULE-Transport, carries 1,900 to 2,400 pounds of equipment and backpacks for dismounted infantry squads. It also has the mobility needed to follow squads in complex terrain.

Under terms of the contract, Curtiss-Wright will supply the processing modules to General Dynamics and Rockwell Collins for integration into the ICS system. The initial order is for more than 1,000 modules with deliveries scheduled to begin during the second quarter of 2008. General Dynamics and Rockwell Collins were jointly awarded a contract by The Boeing Company and Science Applications International Corporation to accelerate technology development of the Integrated Computing System in 2005. By March 2007, the team had designed, built, tested and delivered the first ICS unit for use in an FCS mobile platform.

Curtiss-Wright Controls
Embedded Computing
Leesburg, VA.
(703) 779-7800.
[www.cwcembedded.com].

General Dynamics C4 Systems
Scottsdale, AZ.
(480) 441-3033.
[www.gdc4s.com].

Rockwell Collins
Cedar Rapids, IA.
(319) 295-1000.
[www.rockwellcollins.com].

Raytheon-Led Team Demos Technique for Growing Semi Compounds on Silicon

A Raytheon-led team has accomplished a key step in demonstrating that affordable, high-performance circuits for military applications can be produced by growing semiconductor compounds directly on silicon. Demonstrating this technique is part of a $6.5 million contract awarded by the Office of Naval Research and funded by the Defense Advanced Research Projects Agency. It is a critical building block contributing to the ultimate success of DARPA's Compound Semiconductor Materials on Silicon, or COSMOS, program.

According to Raytheon, selective placement of semiconductor compounds on silicon is an important achievement because it proves that optimal circuit performance can be produced through a heterogeneous, high-yield, monolithic integration process. Teaming with Raytheon IDS on the COSMOS project are Raytheon Systems Limited in Glenrothes, Scotland; Teledyne Scientific Imaging Company in Thousand Oaks, CA.; MIT in Cambridge, MA.; Paradigm Research LLC in Windham, NH; IQE in Bethlehem, PA.; Soitec in Grenoble, France; and Silicon Valley Technology Center in San Jose, CA.

Raytheon
Waltham, MA.
(781) 522-3000.
[www.raytheon.com].

BAE Systems Anti-Missile Decoy Tested on F/A-18 E/F Super Hornet

The U.S. Navy has completed developmental testing of a BAE Systems fiber-optic towed decoy, and has begun operational tests on the F/A-18 E/F Super Hornet (Figure 2). The decoy is a key part of a system that will better protect military aircraft against enemy missiles. The AN/ALE-55 towed decoy is part of the Integrated Defensive Electronic Countermeasures (IDECM) radio frequency countermeasures system. The Navy system provides a highly effective electronic warfare defense against missiles guided by radio frequency. Operational deployment on U.S. Navy F-18s is scheduled for December 2009.

The AN/ALE-55 consists of an onboard electronic frequency converter (EFC) and the fiber-optic towed decoy. The EFC

Figure 2
An F/A-18F Super Hornet aircraft assigned to Strike Fighter Squadron One Zero Two fuels an F/A-18E Super Hornet aircraft from Strike Fighter Squadron Two Seven during an exercise while over the Bay of Bengal last September.

converts radio frequencies to light for transfer through a fiber-optic line to the decoy. IDECM links the aircraft's expendable countermeasures, radar warning system, mission computer and radio-frequency countermeasures system into a unified defensive suite.

BAE Systems
Nashua, NH.
(603) 885-4321.
[www.baesystems.com].

Smiths Detection Selects Parvus Subsystem for Chem/Bio Shelter

Smiths Detection has awarded Parvus an IQID contract extending out to 2016 for DuraCOR 810 processor subsystems in connection with Smiths Detection's Chemical Biological Protective Shelter (CBPS). Smiths Detection has specified the Parvus DuraCOR 810 as the central computing unit (CPU) for its CBPS environmental control system. CBPS shelters provide medical personnel and soldiers a highly mobile, self-contained collective protection system. With a contamination-free, environmentally controlled working area, these shelters serve medical combat services and combat service support personnel as mobile medical aid stations, field command posts or emergency facilities.

Deployed across various unmanned and manned aircraft, ground vehicle and naval installations, the rugged DuraCOR 810 (Figure 3) is an open-architecture solution for military/civil Command, Control, Communications, Computer, Intelligence, Surveillance and Reconnaissance (C4ISR) applications. It is designed to survive harsh mobile environmental conditions experienced under MIL-STD-810F, including extreme temperatures, shock/vibration and ingress, as well as power surge and voltage requirements of MIL-STD-1275D and MIL-STD-704E.

Figure 3
Parvus' DuraCOR 810 system is designed to survive harsh mobile environmental conditions experienced under MIL-STD-810F, including extreme temperatures, shock/vibration and ingress, as well as power surge and voltage requirements.

Parvus
Salt Lake City, UT.
(801) 483-1533.
[www.parvus.com].

General Dynamics Inks Deal to Provide Crypto Technology for Battlefield Nets

General Dynamics C4 Systems has been awarded a $6.5 million contract option to produce Engineering Design Models of the Advanced Cryptographic Module (ACM) for the U.S. Army's Programmable Objective Encryption Technologies (POET) program, following a recent successful Critical Design Review. This option modifies a contract initially awarded in August 2006 and brings the total contract value to $11.5 million.

With the critical design review phase completed, the program is on schedule to deliver the embedded communications capability. The POET program is aligned with the National Security Agency's Cryptographic Modernization Initiative, and will enable high-data-rate, multi-level security for voice, video, data and imagery from a variety of military equipment and networks including U.S. Navy multi-band terminals, U.S. Air Force advanced broadband terminals and U.S. Army High Capacity Communications Capability terminals. The Engineering Design Models are used to demonstrate a subset of cryptographic functions and features.

General Dynamics C4 Systems
Scottsdale, AZ.
(480) 441-3033.
[www.gdc4s.com].

Lockheed Martin Taps VMETRO Data Recorders for F-35 Development

Lockheed Martin has awarded VMETRO a contract to supply Vortex Data Recording systems to support Lockheed Martin's work on the F-35 Lightning II test laboratory. The Data Recording systems are based on VMETRO's Vortex VME Open Data Recording platform. The Vortex system will be incorporated into Lockheed Martin's instrumentation and test plan for Lightning II. The award value exceeds $660,000. Delivery will occur in 2008.

Figure 4
Lieutenant Col. James Kromberg, 461st Flight Test Squadron director of operations, adjusts his helmet as he prepares to fly the F-35 Lightning II earlier this year. Colonel Kromberg's test flight marks the first time a military pilot flew the F-35.

The F-35 Lightning II (Figure 4) Program—also known as the Joint Strike Fighter Program—is the next-generation strike fighter bringing cutting-edge technologies to the battlespace of the future. The System Development and Demonstration (SDD) phase of the F-35 JSF program started with the signing of the SDD contract in October 2001. First flight occurred in 2006. Delivery of production aircraft is scheduled to begin in 2010. During the SDD phase, 19 aircraft will be produced and tested for safety and effectiveness, and to verify the product the Lockheed Martin F-35 team proposed. The JSF program is slated to produce a total of 2,593 aircraft for the United States' and United Kingdom's armed forces, and as many as 2,000 additional F-35s for other allied nations.

VMETRO
Houston, TX.
(281) 584-0728.
[www.vmetro.com].

COTS Websites

www.vdc-corp.com

Venture Development Corp.'s Site Boasts Research on Embedded and More

Focused market research on this industry we call the military electronics and embedded computer market is hard to find. Few of the large—or even the small—market research firms cover this area. One exception is the technology market research and strategy firm Venture Development Corp. (VDC). VDC was founded in 1971 by graduates of the Harvard Business School and the Massachusetts Institute of Technology. The firm boasts over 30 years of experience in providing market research, strategic analysis and consulting services to technology companies worldwide. Its strength, according to VDC, is their ability to bring multi-disciplinary capabilities in the areas of technology, economics, finance, engineering and manufacturing to bear on a problem.

Among the market segments it covers is the military embedded market. VDC's studies of this marketplace emphasize configurations, technologies and applications utilizing merchant computing elements, identifying and suggesting strategies for dealing with issues such as sustainment, technology insertion and technology refresh. VDC sells a variety of multi-client market research reports on embedded systems in military and aerospace applications centered on both the North American merchant market and the European Merchant Market.

Venture Development Corp. (VDC)
Natick, MA. (508) 653-9000.
[www.vdc-corp.com].

Special Feature

Ethernet Switches for Military Apps

Ethernet Switch Boards Blend Network and Fabric Duties

Advances in switched Ethernet technology—in both Gbit and 10 Gbit flavors—are solving the dual needs of networking and real-time fabric interconnect solution in a growing number of military systems.

Jeff Child,
Editor-in-Chief

Until recently, Ethernet's main role was as a control plane solution. Now, thanks in part to the emergence of rugged 10 Gbit Ethernet products, Ethernet is now finally fast enough for data-plane use. Military system designers are now putting 10 Gbit Ethernet to work as a "fat pipe" to move data between subsystems. Military systems that need to pump data into a server farm, for example, for further processing and analysis are looking to 10 Gbit Ethernet as the interconnect linked directly into the server network.

Ethernet is being used as an interconnect fabric in compute-intensive applications like sonar, radar, or any application that networks sensor arrays together. This often means bridging to other protocols in electronic warfare (EW) or combat systems to move data from subsystem to subsystem or from box to box. Ethernet is being used to bring sensor data into other systems—as an alternative to other less common protocols like FPDP, Fibre Channel, or proprietary schemes. There's even a backplane standard for Ethernet released by the IEEE last year. The new standard, IEEE 802.3ap-2007, specifically targets backplane Ethernet applications. See sidebar "Ethernet Over Backplanes Now Standardized."

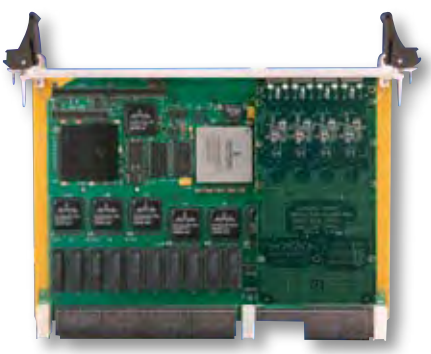


Figure 1

The VPX6-684 FireBlade II from Curtiss-Wright is a high-density 6U VPX Gbit Ethernet multilayer switch/router board designed for rugged embedded aerospace and defense applications. It's available with 12, 20 or 24 Gbit Ethernet ports and up to 4x10 Gbit Ethernet ports.

Boasting higher levels of performance and capability than the other military I/O technologies, Ethernet is now taking on much more data-intensive and time-critical applications. Both 1 Gbit and 10 Gbit Ethernet can now—when properly implemented with offload technology—provide a highly deterministic, high-performance fabric suitable for the most demanding real-time applications. Meanwhile, in a more traditional networking role, Ethernet is being deployed in multilayer switches with dual IPv4 and IPv6 forwarding to support the DoD's sweeping plans to leverage the benefits of IPv6 (Internet Protocol version 6).

A Rich Set of Switch Products

Serving both the real-time interconnect and traditional networking needs, the embedded board industry offers a rich set of rugged Ethernet switch boards. Rugged Ethernet switch boards are available from several vendors including ACT/Technico, AdvancedIO Systems, Concurrent Technologies, Continuous Computing, Curtiss-Wright, GE Fanuc, Kontron America, Performance Technologies, One Stop Systems and Parvus.

Ethernet switches are among the products rounding out the ecosystem of the emerging VPX form factor. A fabric-based next-gen VME form-factor, VPX is aimed squarely at military systems. For its part, Curtiss-Wright Controls Embedded Computing offers a high-density 6U VPX Gbit Ethernet multilayer switch/

Get Connected
with companies mentioned in this article.
www.cotsjournalonline.com/getconnected

router board designed for rugged embedded aerospace and defense applications.

The VPX6-684 FireBlade II (Figure 1), available with 12, 20 or 24 Gbit Ethernet ports and up to 4x10 Gbit Ethernet ports, is ideal for system integrators architecting secure high-performance IPv4/v6 Intra-Platform Networks (IPNs). The board operates as either a fully managed or an unmanaged switch/router. The VPX6-684 FireBlade II is ideal for use in applications that require high levels of security. When used as a Unified Threat Management (UTM) router, the VPX6-684 FireBlade II provides strong perimeter defense via an ICSA-certified firewall. Additional security features supported by the board include Access Control List (ACL) filtering, Network Address Translation (NAT), Virtual Private Network (VPN) with tunneling support (IPSec/L2TP), IPv6 ESP/AH payloads and Encryption/ Decryption/Authentication support.

Moving Toward IPv6 Nets

As the DoD moves toward upgrading to IPv6 this year, support of IPv6 has become a core requirement for network-centric warfare. Feeding that need, GE Fanuc's NETernity GBX410 is a fully managed (Layer 2/3) Gigabit Ethernet switch designed to meet the most demanding requirements for network switching in tactical applications. This Gigabit switch is available in both air- and conduction-cooled formats and features a non-blocking shared memory architecture. This provides a 72 Gbit/s core offering full wire speed performance with minimal latency on all ports simultaneously.

The GBX410 has comprehensive management capabilities that include VLANs, Link Aggregation, Spanning Tree, IPv4, IPv6, Traffic Policing, Quality of Service (QoS), Guaranteed Bandwidth and SNMP. The GBX410 can be expanded to a 32-port non-blocking solution by connecting two GBX410s together via the integral 10 Gigabit uplink ports. The GBX410 provides optional optical expansion through a separate Optical Expansion Board. All twelve rear ports can be converted to optical outputs to give sixteen ports of Gigabit, either 1000 Base-SX or 1000 Base-LX, and two port of 10 Gigabit, either 10G Base-SR or 10G Base-LR. Onboard built-in test (BIT) ensures the GBX410 can be easily linked with other boards to provide integrated system-level health monitoring and diagnostics.

Figure 2

A switched Ethernet product, along with other subsystems, was selected by Lockheed Martin's Littoral Ships & Systems business for the control system in the Non-Line-Of-Sight Launch System (NLOS-LS) platform commissioned by the U.S. Army. NLOS-LS is scheduled to be part of "spin-out one" within the U.S. Department of Defense's Future Combat Systems (FCS) initiative. The GE Fanuc processing subsystem selected by Lockheed Martin comprises an adapted version of one of the company's standard rugged enclosures; together with a Compact PCI 6U CP1A single board computer fitted with an I/O daughter card PMC; a CPX24 rugged managed Gigabit Ethernet switch; and a Radstone MFIO (Multi Function I/O) board.

NLOS-LS is being developed for the U.S. Army by Netfires LLC, a joint venture between Lockheed Martin and Raytheon. It uses a common vertical launch Container Launch Unit (CLU) comprising 15 missile launch chambers. It also has integrated command and control equipment to support the deployment of the Precision Attack Missile (PAM). The CLU is platform-independent and is transportable by truck (shown), plane, helicopter or ship. The CLU can be fired from a platform or the ground, and can operate in an autonomous mode.

Growing Acceptance in Mil Programs

There's a growing number of military programs that are putting switched Ethernet to work as an interconnect fabric. Switched Ethernet is being used, for example, as an interconnect for the upgraded electronics on BAE Systems' Bradley Fighting Vehicle Program (Figure 1). Last summer BAE awarded LaBarge a contract to continue to produce the Ethernet Switch Unit (ESU) for its A3 Bradley Combat Systems vehicles. The ESU functions as a router and a switch, making local forwarding decisions to devices operated in the vehicle's LAN (local area network). The A3 upgrade version of the Bradley features an advanced digital architecture that integrates communica-

Ethernet Over Backplanes Now Standardized

Ethernet was designed for connecting host computers together through a Local Area Network (LAN). The most common type of Gbit Ethernet connection is defined in IEEE 802.3 as 1000BASE-T and uses the ubiquitous RJ45 modular plug that is present on nearly every laptop and workstation shipping today. This type of connection supports autonegotiation between 10, 100 and 1000 Mbit/s data rates and maintains backward compatibility with slower Ethernet and Fast Ethernet devices.

In addition to the basic copper twisted-pair interface, Ethernet defines a range of external interfaces using fiber and copper, and also defines several different ways for the internal Media Access Controller (MAC) to connect to the Physical Medium Attachment (PMA) and Physical interface (PHY). For Gbit Ethernet, the most common internal interface has been Gigabit Media Independent Interface (GMII) and a serialized variant called SGMII. Although not standardized by IEEE 802.3, SGMII is widely used by semiconductor manufacturers as a PHY interface due to its low pin count.

When military embedded systems developers first started to look at Ethernet as an internal chassis interconnect, the most important goal was to achieve Gigabit Ethernet speeds with a minimum number of signal pins. The most efficient approach uses a single 1.25 Gbit/s signal in each direction, but none of the existing Gigabit Ethernet standards quite fit the bill. 1000BASE-CX uses a single 1.25 Gbit/s signal, but specifies 150 ohm cabling instead of 100 ohm backplane traces and is designed for longer cabling lengths. SGMII can be used with a single 1.25 Gbit/s data signal in each direction, but is not an IEEE standard and is not completely specified for backplane usage. In the end, tailored versions of both 1000BASE-CX and SGMII were adapted and used as the basis for Gigabit Ethernet backplane standards by PICMG and VSO.

Last year, the IEEE released a new standard, IEEE 802.3ap-2007, which specifically targets backplane Ethernet applications by adding three new physical interfaces: 1000BASE-KX, 10GBASE-KX4 and 10GBASE-KR. 1000BASE KX is very similar to the 1000BASE-CX and SGMII variants that are in use today and standardizes the use of a single 1.25 Gbit/s pair in each direction over a backplane. 10GBASE-KX4 and -KR provide 10GbE links over a backplane, using either four XAUI 3.125 Gbit/s signal pairs (KX4) or a single 10.3125 Gbit/s signal pair (KR) in each direction. Both links provide 10 Gbits/s of data after encoding overhead. VITA 41.8 is based on the KX4 standard, using the same 3.125 Gbit/s link speed already used on the backplane by Serial RapidIO and Aurora but with the advantages of the Ethernet ecosystem.

— Andy Reddig, Tek Microsystems

tions equipment, digital sensors, battle management systems, embedded diagnostic and training systems.

IP-based Monitoring and Networking

Ethernet-based IP technology is being employed in Raytheon's SSDS Mk 2 (Ship Self-Defense System) program. The SSDS MK 2 Modification 1 is used on aircraft carrier USS Ronald Reagan. Raytheon uses Performance Technologies' Advanced Managed Platform IP-comms platform to provide sophisticated remote monitoring capabilities, and an IP-based networking platform for the SSDS system. The Performance Technologies IP-based platform solution features an Intelligent Shelf Manager (a self-contained computer) that provides sophisticated remote monitoring capabilities, and an IP-based networking platform for the SSDS system.

The SSDS MK2 system relies on distributed off-the-shelf embedded computers that provide automated detection through engagement capability, coordination and control of weapons and situational awareness command and control at the battle group level. Follow-on development will include enhanced air and surface capabilities for slow moving targets as well as organic training capability.

A switched Ethernet product, along with other subsystems, was se-

lected by Lockheed Martin's Littoral Ships & Systems business for the control system in the Non-Line-Of-Sight Launch System (NLOS-LS) platform (Figure 2) commissioned by the U.S. Army. NLOS-LS is scheduled to be part of "spin-out one" within the U.S. Department of Defense's Future Combat Systems (FCS) initiative.

Embedded 10GbE Adaptors

Embedded adaptor cards are also joining the 10 Gbit Ethernet band wagon. An example is an XMC product (Figure 3) from Critical I/O. Designed for military and avionics applications, it incorporates the company's Silicon Stack technology, which offloads TCP/IP protocol stack processing to hardware, thus allowing wire-speed transfers, minimal host processor overhead, very low latency and solid determinism. As a result, the 10GbE XGE interfaces from Critical I/O permit users of high-performance systems to benefit from the low-cost, interoperability and networking capabilities of Ethernet, even in such applications as radar, sonar, flight simulation and scientific applications.

According to the company, 10GbE holds the promise of providing an order of magnitude increase in performance, offering an attractive alternative to other more specialized data networking technologies, such as InfiniBand and Serial RapidIO. The problem users run into, however, has to do with the software-intensive nature of Ethernet's TCP/IP protocol stack.

Many embedded systems have struggled to keep up with the stack processing associated with 1GbE connections, so dealing with 10GbE presents 10 times the challenge. The Silicon Stack technology is used as a solution to offload protocol processing to silicon and reduce host processor loading so as to deliver true 10 Gbit performance. The XGE 10Gb family is currently available in an XMC form factor with dual 10GbE ports, and employs an 8-lane PCI Express host bus interface. AMC and PMC versions are also planned. Native support for IPv4 and IPv6 is included. ▮▮

Figure 3

Critical I/O's 10 Gbit Ethernet XMC adaptor card features technology that offloads TCP/IP protocol stack processing to hardware, thus allowing wire-speed transfers, minimal host processor overhead, very low latency and solid determinism.

ACT/Technico
Ivyland, PA.
(215) 956-1200.
[www.acttechnico.com].

AdvancedIO Systems
Vancouver, British Columbia
Canada.
(604) 331-1600.
[www.advancedio.com].

Concurrent Technologies
Woburn, MA.
(781) 933 5900.
[www.gocct.com].

Continuous Computing
San Diego, CA.
(858) 882-8800.
[www.ccpu.com].

Critical I/O
Irvine, CA.
(949) 553-2200.
[www.criticalio.com].

Curtiss-Wright Controls
Embedded Computing
Leesburg, VA.
(703) 779-7800.
[www.cwcembedded.com].

GE Fanuc Intelligent Platforms
Charlottesville, VA.
(800) 368-2738.
[www.gefanucembedded.com].

Interface Concept
Briec de l'Odet, France.
+33 (0)2 98 57 30 30.
[www.interfaceconcept.com].

Kontron America
Poway, CA.
(858) 677-0877.
[www.us.kontron.com].

Performance Technologies
Rochester, NY.
(585) 256-0200.
[www.pt.com].

One Stop Systems
Escondido, CA.
(760) 745-9883.
[www.onestopsystems.com].

Parvus
Salt Lake City, UT.
(801) 483-1533.
[www.parvus.com].

Special Feature

Ethernet Switches for Military Apps

10 Gbit Ethernet Fuels Network-Centric VXS Systems

Fabrics like RapidIO provide the speedy interconnect at the foundation of many new embedded form factors. But military system designers are now eyeing 10 Gbit Ethernet, which has the potential to meet both control and data plane requirements.

Andrew Reddig, President and CTO
TEK Microsystems

High-performance military embedded applications have pushed aside traditional bus architectures for switched fabric interconnects. All of the new form factors—VXS, VPX, XMC, ATCA and MicroTCA—embrace the use not only of fabrics but also of fabric-agnostic architectures, allowing systems integrators to select the right fabric for their application and in some cases to mix different fabrics within the same system. While the first set of standards focused on "embedded" fabrics such as RapidIO, the use of Gbit Ethernet and now 10 Gbit Ethernet (10GbE) is the subject of several new VITA 41 standards, with 10GbE having the potential for both control and data plane requirements.

The ANSI/VITA 41.0 (VXS) base standard defines a common set of mechanical, power and backplane requirements and allows board vendors and systems integrators to choose from a menu of fabrics when selecting features for payload and switch cards. The options available within the VXS ecosystem are shown in Table 1.

Board vendors can provide payload and switch cards within the VXS framework that support specific interconnects, or by using FPGA-based endpoints can often provide a range of choices using the same physical hardware with different IP cores. This has resulted in a wide range of options for systems integrators building deployed VXS solutions today.

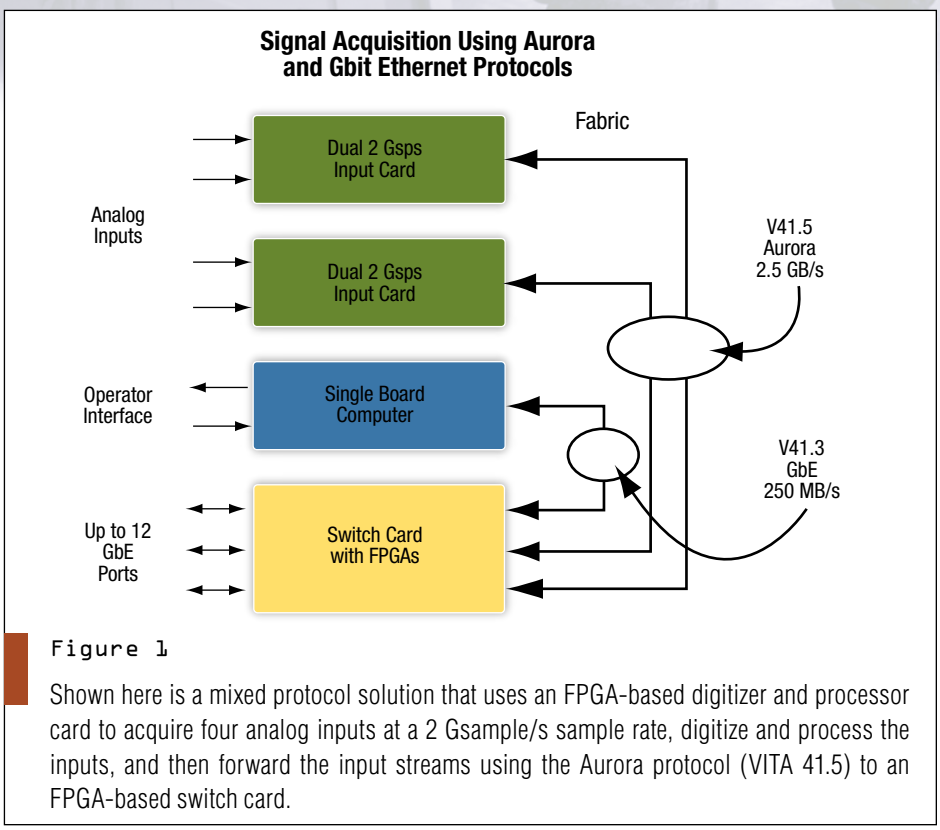


Figure 1

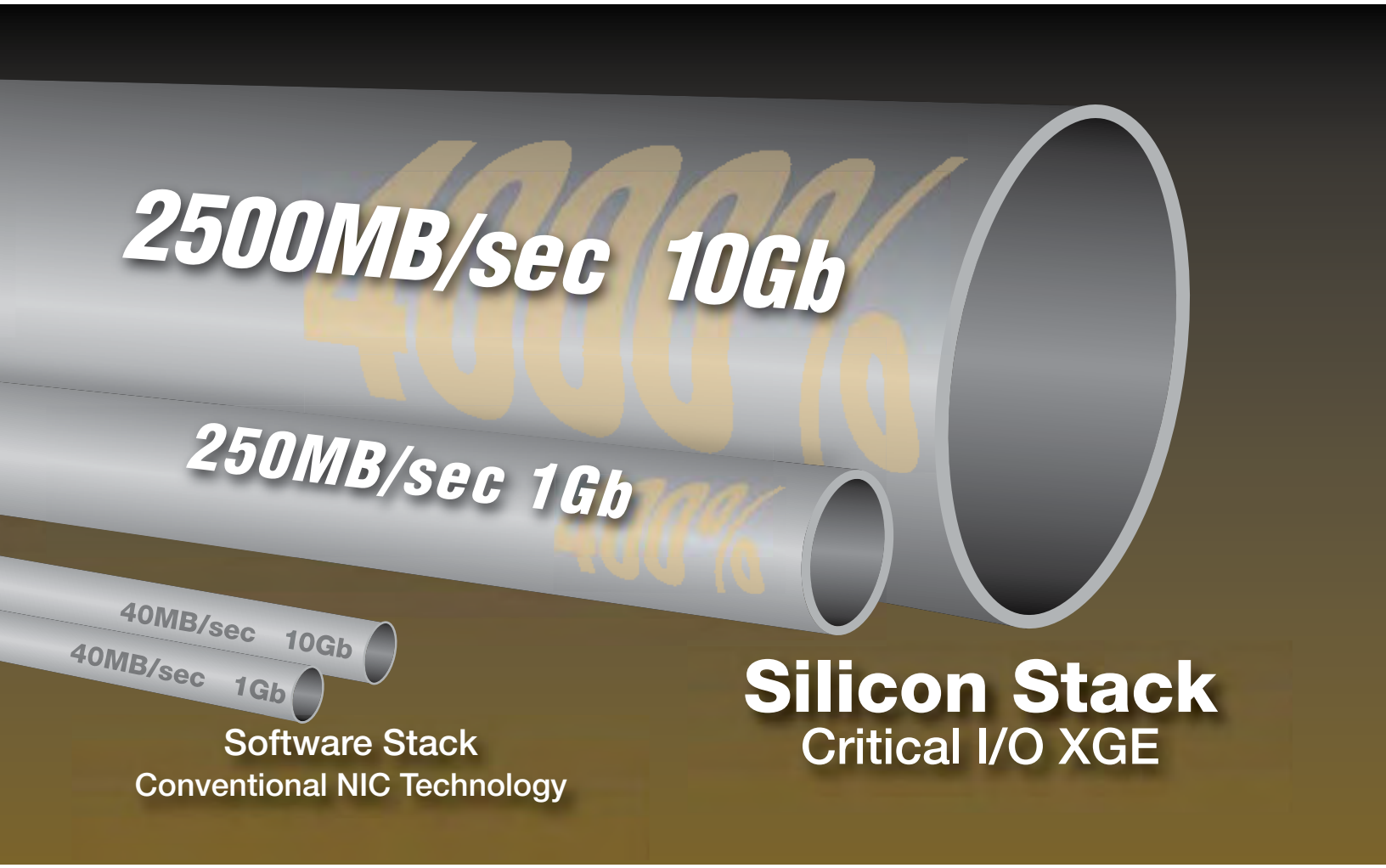
Shown here is a mixed protocol solution that uses an FPGA-based digitizer and processor card to acquire four analog inputs at a 2 Gsample/s sample rate, digitize and process the inputs, and then forward the input streams using the Aurora protocol (VITA 41.5) to an FPGA-based switch card.

One Size Does Not Fit All

One advantage of the VXS architecture is that the interconnect protocol being used is in essence an agreement between the two endpoints, usually a payload card and a switch card. This allows the systems integrator to pick and choose different interconnect protocols within the same system, provided that the board vendors have the flexibility to support multiple protocols. Typically, this implies an FPGA-based endpoint, which has built-in flexibility through the use of different IP cores within the FPGA device.

An example of a mixed protocol solution using currently available technology is shown in Figure 1. This application uses an FPGA-based digitizer and processor card to acquire four analog inputs at a 2 Gsample/s sample rate, digitizes and processes the inputs, and then forwards the input streams

Which Way do You Want Your 10Gb Ethernet?



Silicon Stack Technology from Critical I/O. 10Gb Ethernet at Wire Speed.

[**Problem**] You're expecting 10Gb Ethernet to deliver a whole lot more performance to your embedded system. But what if you invest in it and get no gain at all? The performance of nearly all existing 1Gb applications are limited by the software overhead associated with the TCP/IP protocol stack. This bottleneck is in the software stack, not the network hardware. So, simply upgrading to 10Gb pipes will not improve your system's performance.

[**Solution**] Unlike conventional Ethernet interfaces or processor-based "offload" products, Critical I/O's Silicon Stack technology eliminates this inherent bottleneck by offloading protocol processing to silicon; thereby achieving sustained line-rate performance, microsecond latency, and rock-solid deterministic behavior. And, Silicon Stack is 100% compliant with Ethernet standards, allowing you to leverage existing applications and hardware.

XGE Silicon Stack Ethernet
vs. Software-based Stack

	Software Stack		Silicon Stack	
	1Gb	10Gb	1Gb	10Gb
Throughput max sustained rate in MBytes/sec	40 varies with protocol		250	2500
Host Overhead	Very High		Very Low	
Latency	125 µsec		12 µsec	5 µsec
Determinism typical variation	Horrible ± 200 µsec		Rock Solid ± 1 µsec	
Reliability	Poor when under heavy load		Excellent under all load conditions, no dropped data	

CRITICAL IO

www.criticalio.com

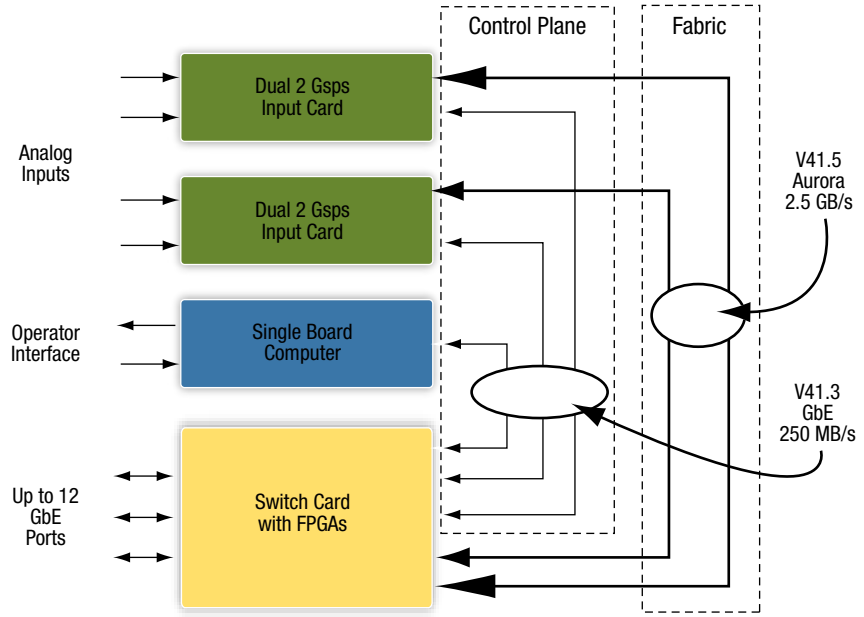


Figure 2

In this example the system architecture is simplified by reserving the fabric for streaming data and isolating control traffic to the 41.6 control plane.

using the Aurora protocol (VITA 41.5) to an FPGA-based switch card. The switch card performs additional processing and traffic management and forwards snapshots of the processed data both to a local SBC using Gbit Ethernet (VITA 41.3) and also to up to a dozen external processors using front panel Gbit Ethernet interfaces.

The Aurora protocol was selected for the input-to-switch interconnect for both raw throughput and FPGA efficiency. Aurora typically provides 99% or better link utilization, versus 87% typically found with general-purpose fabric interfaces, and is also very resource efficient within the FPGA devices at each end. The end result is that more FPGA gates are available for processing, raising the overall effectiveness of the system in terms of processing within a given set of size, weight and power constraints.

Gbit Ethernet was selected for the switch-to-processor interconnect because it meets the lower throughput requirements for processed data and is available on a wide range of Single Board Computers (SBCs) using VITA 41.3. Gbit Ethernet also offers a common network interface for both within-the-box and outside-the-box communications, making the system quicker to prototype and also easier to scale up or down by adding additional SBC resources.

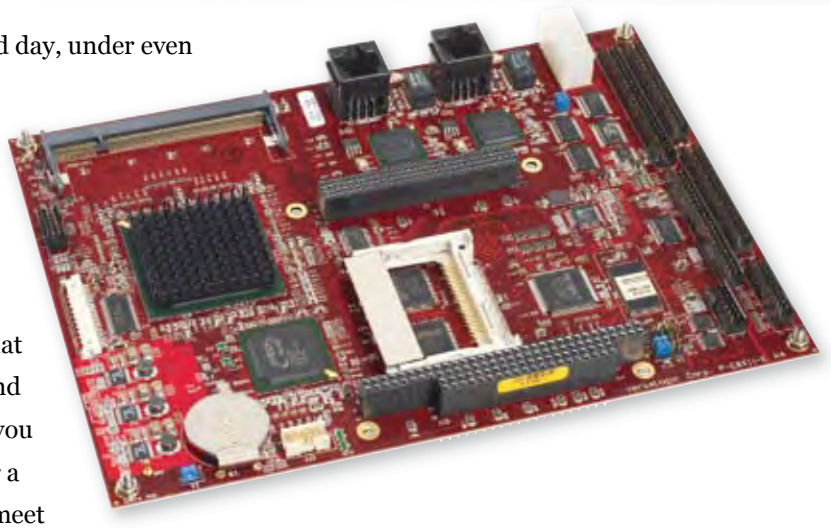
Separate Control Plane

The recently finalized VITA 41.6 standard makes these trade-offs easier to make by providing an independent Gbit Ethernet fabric between payload and switch cards using a separate set of P0 pins on the payload cards. This allows board vendors to support a Gigabit Ethernet control plane while still supporting the fabric of their choice on the high-speed fabric links. In the above example, the system architecture can be simplified by reserving the fabric for streaming data and isolating control traffic to the 41.6 control plane as shown in Figure 2. Because Xilinx Virtex 5 FPGAs have built-in support for Gigabit Ethernet, adding a separate control plane actually lowers FPGA resource usage. By enabling a direct network connection on each payload card,

When You Design for the Extreme Choose Your Partner Wisely

Did we mention "Reliability" is our middle name?

Industrial equipment needs to perform flawlessly, night and day, under even the most extreme conditions. Whether designing for the manufacturing floor, clean room or the field, you can depend on VersaLogic to deliver the highest quality embedded computer products, from prototyping and design-in, through years of product production. We design our boards for high reliability and long-term availability, then run them through exhaustive quality tests, ensuring that we deliver only the best. And with our world class service and five year availability guarantee, we'll always be there when you need us. Whether you need one of our standard products or a customized version, our skilled technical staff will work to meet your exact requirements.



Contact us to find out how for more than 30 years we've been perfecting the fine art of extra-ordinary support and on-time delivery: One customer at a time.

1.800.824.3163
1.541.485.8575
www.VersaLogic.com/ind

VERSALOGIC CORPORATION

SBCs and external hosts can now communicate directly with every card, making the overall system more network-centric and improving system manageability.

While Gigabit Ethernet offers a lot of advantages, as a VXS fabric choice it still has one huge disadvantage: raw speed. Because VITA 41.3 uses 1.25 Gbit/s links, the theoretical throughput of a fully implemented system is only 40% of what can be achieved with Serial RapidIO or Aurora. In addition, while 41.3 allows payload cards to imple-

Signal Acquisition with 10 Gigabit Ethernet

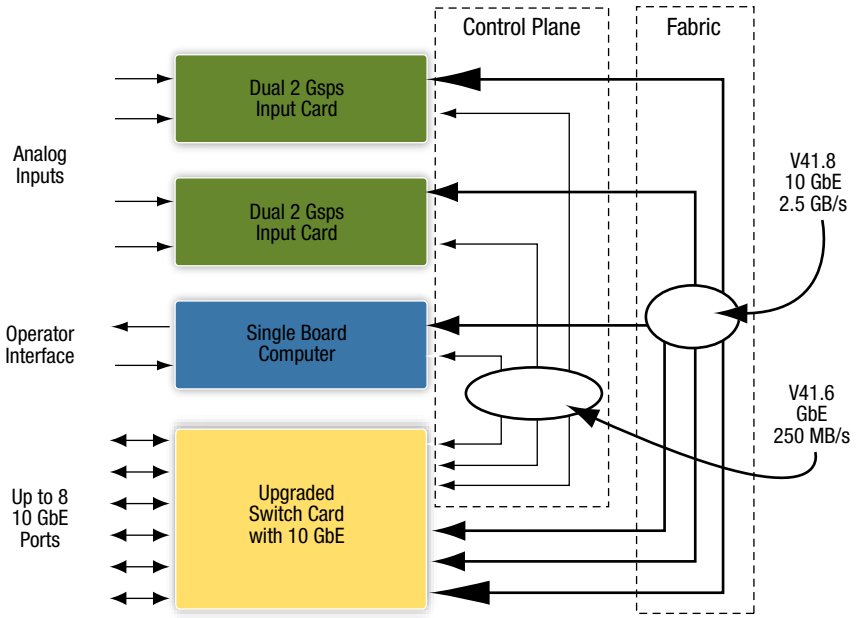


Figure 3

The VXS shown earlier is updated here as a fully network-centric architecture. It uses VITA 41.6 for a Gbit Ethernet control plane and VITA 41.8 for a 10 Gbit Ethernet data plane.

Fabric Choices in VXS Today

Standard	Protocol	Serial Bit Rate	Links per Payload Card	Throughput per Payload Card
ANSI/VITA 41.1	InfiniBand	2.5 Gbits/s	2 x 4 lanes	2.0 Gbytes/s
ANSI/VITA 41.2	Serial RapidIO	3.125 Gbits/s	2 x 4 lanes	2.5 Gbytes/s
VITA 41.3	Gigabit Ethernet (using P0 fabric pins)	1.25 Gbits/s	8 x 1 lane	1.0 Gbyte/s
VITA 41.4	PCI Express	2.5 Gbits/s	2 x 4 lanes	2.0 Gbytes/s
VITA 41.5	Aurora	3.125 Gbits/s	2 x 4 lanes	2.5 Gbytes/s
VITA 41.6	Gigabit Ethernet (using P0 sideband pins)	1.25 Gbits/s	2 x 1 lane	250 Mbytes/s
VITA 41.8	10GbE Fabric	3.125 Gbits/s	2 x 4 lanes	2.5 Gbytes/s

Table 1

The ANSI/VITA 41.0 (VXS) base standard defines a common set of mechanical, power and backplane requirements. It allows board vendors and systems integrators to choose from a menu of fabrics when selecting features for payload and switch cards. The options available within the VXS ecosystem are listed here.

Real Cost Savings in MicroTCA™ Begins with Performance Technologies.

Finding the cost savings promised with MicroTCA™ may seem like trying to pull a rabbit out of a hat. And while others may discuss low cost, Performance Technologies' revolutionary, 1U highly integrated MTC5070 delivers the true promise of MicroTCA in an affordable platform. With **volume prices under $2000,** this rugged platform is available right now for your most demanding applications.

Industry Firsts for a 1U MicroTCA Chassis:

- Superior Front-to-Back Cooling
- Innovative New Architecture Minimizes Cost and Profile
- Highly Integrated Infrastructure includes Ethernet Switch, PCI Express® Switch, Dual 1 GbE Uplinks, and Platform Management
- Low-cost Enterprise-class Removable Power Supply (AC or DC)

Additional World-Class Features Include:

- 6 AMC Slots (Supports Mid or Full, Single or Double Sizes)
- Low Profile (1U), High Density
- Ruggedized Steel Chassis
- Completely MicroTCA.0 Compliant and Designed for NEBS

It's no longer an illusion. Call Performance Technologies today to turn your MicroTCA project into a deliverable, cost-effective reality.

For more information, download our white paper today:

MicroTCA™
Flexible, Scalable, and Cost-Effective Systems

www.pt.com/uTCA

PERFORMANCE TECHNOLOGIES

Phone: 585.256.0200 ◆ www.pt.com/mtc5070 ◆ E-mail: info-request@pt.com

ment up to eight Gbit Ethernet links, in reality the overhead of multiplexing separate links makes this option unrealistic. Typical implementations include two links per payload slot, resulting in throughput that is 10% of other fabric options.

By using a 10 Gbit Ethernet fabric, being standardized for VXS as VITA 41.8, systems can leverage commercially available 10 Gbit technology to fully address the limitations of Gbit Ethernet. First of all, VITA 41.8 is based on the 10GBASE-KX4 standard, which uses a raw serial bit rate of 3.125 Gbits/s, which is as fast or faster than RapidIO-based VXS implementations. Second, a 10 Gbit Ethernet link uses four serial pairs for each link, resulting in two logical links per payload card instead of eight Gigabit links. This allows systems to easily use both single and dual star topologies without any unnecessary overhead on the payload card.

Effective use of 10 Gbit speeds depends on an ecosystem of solutions that provides efficient solutions for both switches and endpoints. In this area, 10GbE potentially offers significant advantages due to the need within the commercial marketplace for the high-performance features that are critical for military embedded applications such as TCP offload and RDMA support. Native 10GbE support is currently available for both embedded and x86 class processors, and FPGA IP cores are available for FPGA-based endpoints. Over time, it seems clear that 10GbE endpoints and switches will become as ubiquitous as Gigabit Ethernet is today, allowing board vendors to leverage a broad ecosystem for 10GbE solutions that are both power and space efficient.

Truly Network-Centric Embedded Computing

By using VITA 41.6 for a Gbit Ethernet control plane and VITA 41.8 for a 10 Gbit Ethernet data plane, the original VXS system can be updated to a fully network-centric architecture as shown in Figure 3. Because the payload cards are FPGA-based, this technology refresh can be implemented by upgrading the IP cores used in the payload cards and installing a VITA 41.8-compliant switch card.

This architecture brings with it all of the inherent advantages of an Ethernet-based system. Software interfaces are familiar and well defined, and can easily be implemented on any type of host computer and operating environment. Control and data traffic can be transparently segmented between the control and data planes through routing on the switch card, or traffic can be intermixed on the fabric network if desired. External resources can easily be integrated into the network using 1 or 10GbE ports as required.

The end result of 10GbE technology will be a more network-centric view of military embedded VXS-based systems. The system architecture easily scales to include external sensor inputs and processing outputs all using common network interfaces. This enables future VXS systems to easily fit into a more network-centric architecture within the deployed platform. ▮▮

TEK Microsystems
Chelmsford, MA.
(978) 244-9200.
[www.tekmicro.com].

DESIGN FOR TIME

It's about *more* than technology,
it's about sustaining technology over time

What part do you play?

Selecting the latest technology is only part of the answer. As the electronics industry's premier distributor, Avnet Electronics Marketing helps you bridge the gap between legacy and leading edge – mil-spec and COTS – obsolescence and sustainability. Our defense/aero team of experts work to protect your design investment, flex your creativity and stretch your product's life expectancy. Avnet provides comprehensive supply-chain and integration services, strategic product intelligence and design support for all your mission-critical projects and applications. Delivering reliable, sustainable solutions from the strength and scale of a trusted industry veteran – ***that's our part.***

How will you DESIGN FOR TIME?

Download our white paper, "The Best Defense Is a Good Offense," at:
www.em.avnet.com/DesignForTime

AVNET® electronics marketing

Accelerating Your Success™

Tech Recon

The FPGA Computing Revolution

FPGAs Ignite Revolution in Military System Design

The impact of FPGAs—as both an embedded computing solution and a system integration solution—is revamping the way the military approaches system development.

Jeff Child,
Editor-in-Chief

Gone are the days when system design meant integrating racks of boards or choosing a board set for a backplane-based solution. Today, as field programmable gate arrays (FPGAs) evolve to ever greater sophistication, complete systems can now be integrated into one or more FPGAs. And now rack and backplane-based systems based on FPGAs offer the compute muscle of yesterday's supercomputers. FPGAs can be configured with data paths crafted specifically for given tasks. Reaping the rewards of this trend are applications ranging from military to high-end industrial and data acquisition.

Those trends got special attention at a luncheon panel discussion earlier this month at the Boston RTECC (Real-Time Embedded Computing Conference). The panel was moderated by this article's author and the topic was "FPGA Computing: Redefining System Design." Comprising this distinguished panel (Figure 1) were Rodger Hosking of Pentek, Ken Karnofsky of The MathWorks, Andy Reddig of TEK Microsystems and Patrick Stover of Annapolis Micro Systems.

Figure 1

The special luncheon panel at last month's Boston RTECC show explored the topic of "FPGA Computing: Redefining System Design." From left to right, Patrick Stover of Annapolis Micro Systems, Andy Reddig of TEK Microsystems. Ken Karnofsky of The MathWorks and Rodger Hosking of Pentek.

Panelists Explore Changing Role of FPGAs

The panelists reflected on how, at one time, FPGAs were used mostly as "glue logic." Now they offer the capability to really define system functionality and carry the heavy processing duties. The panelists talked about how FPGAs have been steadily ramping up their on-chip DSP capabilities, and how today's crop of advanced FPGAs trade off versus DSP chip and General Purpose Processor solutions in terms of solving signal processing problems. Another interesting question posed to the panel was the relevance of reconfigurable computing—where an FPGA enables a system to reconfigure on the fly—and how that compares to configurable computing—where a system can be reconfigured in the field, but that reconfiguration isn't part of the application.

Exemplifying that trend of complete systems that can be crammed into a single FPGA device, Xilinx last month announced its Virtex-5 FXT devices (Figure 2), the industry's first FPGAs with embedded PowerPC 440 processor blocks, high-speed RocketIO GTX transceivers and dedicated XtremeDSP processing capabilities.

The Virtex-5 FXT platform offers the first FPGAs to provide up to two industry-standard PowerPC 440 processor blocks. Each processor, with integrated 32 Kbyte instruction and 32 Kbyte data caches, delivers up to 1,100 DMIPS at 550 MHz. Tightly coupled to the PowerPC440 blocks is a new integrated 5x2 cross bar processor interconnect architecture that provides simultaneous access to I/O and memory.

Figure 2

The Xilinx Virtex-5 FXT devices are the first FPGAs with embedded PowerPC 440 processor blocks, high-speed RocketIO GTX transceivers and dedicated XtremeDSP processing capabilities.

The device includes dedicated master and slave processor local bus interfaces, four DMA ports with separate transmit and receive channels, and a dedicated memory bus interface enabling high-performance, low-latency point-to-point connectivity.

New FPGA-based Mezzanine

Meanwhile, FPGAs have even captured their own form factor spec. The sidebar "VITA 57 Spec Provides Modular FPGA Solution" detailing the new VITA 57 standard, also called the FPGA Mezzanine Card (FMC), addresses these issues. The FMC standard defines an I/O mezzanine module that works intimately with an FPGA.

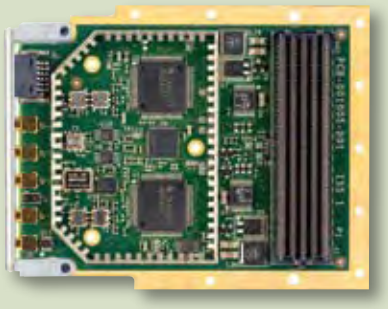
The impact of FPGAs is also fueling a need to rethink the system design process. Capabilities that once could only be done in an ASIC design or microprocessor system can now benefit from the shorter design cycle times and simpler hardware verification processes of an FPGA. The article later in this section entitled "FPGA Trends Fuel Defense Design Organization Rethink" by Altera's J. Ryan Kenny explores that important trend. ▮▮

Altera
San Jose, CA.
(408) 544-7000.
[www.altera.com].

Annapolis Micro Systems Inc
Annapolis, MD.
(410) 841-2514.
[www.annapmicro.com].

VITA 57 Spec Provides Modular FPGA Solution

The new FPGA Mezzanine Card (FMC) specification—VITA 57—defines an I/O mezzanine module designed to work intimately with an FPGA. The standard defines two widths: single and double width. A single-width module measures 69 x 76.5 mm—approximately half the size of a PMC module, and supports a single connector, P1, to the carrier. The double-width module measures 139 x 76.5 mm and can support one or two connectors to the carrier, P1 and P2. The double-width FMC is for applications that require additional bandwidth to the carrier, more front panel space, or a larger PCB area. As is the case with most commercial PMC/XMC modules, most commercial FMCs will be single width.



Figure

The first FPGA Mezzanine Card (FMC/VITA 57) module is VMETRO's ADC510, available in air-cooled and conduction-cooled rugged versions. It integrates two 12-bit 500 MHz A/D chips for use in DSP applications such as SIGINT, ECM, and radar.

VITA 57 provides a choice of two different connectors to interface the FMC to an FPGA on a carrier: a Low Pin Count (LPC) connector with 160 pins and a High Pin Count (HPC) connector with 400 pins. An FMC with the LPC connector can mate with a carrier that utilizes either an LPC or HPC connector. To support the widest range of FMCs, commercial carriers should utilize the HPC connector. The FMC specification was developed to enable FMCs to be supported on a wide range of existing form factors, including but not limited to VME, CompactPCI, VXS, VPX, VPX-REDI, CompactPCI Express, AdvancedTCA and AMC.

The connector was chosen to ensure developers have the functionality and performance they need to allow them to move their I/O to a mezzanine card. The connector is designed to support single-ended and differential signaling up to 2 Gbits/s and signaling to an FPGA's Multi-Gigabit Transceivers (MGTs) up to10 Gbits/s. The LPC connector provides 68 single-ended user-defined signals or 34 user-defined differential pairs, one MGT pair, clocks, a JTAG interface and an I^2C interface to optionally support the base IPMI commands. The HPC provides 160 single-ended user-defined signals or 80 user-defined differential pairs, 10 MGT pairs and additional clocks. Figure 3 shows the first FPGA Mezzanine Card (FMC/VITA 57) module. VMETRO's ADC510, available in air-cooled and conduction-cooled rugged versions, integrates two 12-bit 500 MHz A/D chips for use in DSP applications such as Signal Intelligence (SIGINT), Electronic Counter Measures (ECM) and Radar.

The MathWorks
Natick , MA .
(508) 647-7000.
[www.mathworks.com].

Pentek
Upper Saddle River, NJ.
(201) 818-5900.
[www.pentek.com].

TEK Microsystems
Chelmsford, MA.
(978) 244-9200.
[www.tekmicro.com].

VMETRO
Houston, TX.
(281) 584-0728.
[www.vmetro.com].

Xilinx
San Jose, CA.
(408) 559-7778.
[www.xilinx.com].

Tech Recon

The FPGA Computing Revoltuion

FPGA Trends Fuel Defense Design Organization Rethink

As FPGAs continue to expand system design roles, they're having an impact on how defense industry engineering organizations function and their organizational structure.

J. Ryan Kenny, Mil/Aero Technical Marketing Manager
Altera

With the introduction of 40nm field programmable gate arrays (FPGAs), the design domains of military electronics that can be addressed with programmable logic devices (PLDs) are growing (Figure 1). This is a response to military requirements, as well as a function of the rising cost of new ASIC starts in successive generations of silicon geometry. Functions that were once restricted to ASIC designs or microprocessor systems now benefit from the shorter design cycle times and simpler hardware verification processes of an FPGA.

Although this leads to important efficiencies in military systems design, it also has a fundamental effect on the systems engineering process, as well as the management of engineering organizations in defense programs. By examining several ways that FPGAs are expanding system design roles, there are several conclusions that can be drawn that impact the mix of talent needed in engineering organizations, as well as their organizational structure.

Get Connected
with companies mentioned in this article.
www.cotsjournalonline.com/getconnected

The relationship between military user requirements and commercially available technology is not accidental. A growing number of national militaries are being equipped entirely with off-the-shelf equipment. Likewise, the U.S. military is continually being challenged to leverage commercially available technology into battlefield settings. Today's soldiers that are used to handheld and wireless technology at home, demand similar soldier-to-soldier connectivity in the field.

One particular application example is next-generation airborne sensors. New, larger programmable logic devices offer an ideal solution to integrate flexible circuitry for multiple modes in a productive design flow that allows for simple technical upgrades without reinventing critical IP.

While the number of technical requirements engaging systems engineers cannot be easily summarized, there are four very large initiatives in military electronics technology that are addressed by the larger class of new FPGA devices. These are reductions in size, weight and power (SWaP), common data bus standards ("open systems"), design re-use and anti-tamper technologies.

The simplest approach to reducing SWaP is integrating many subsystems into a single chip. While this can be enabled through robust systems engineering processes and workflow controls, it increases the importance of open systems design and anti-tamper technologies for FPGAs. In order to see improvements in efficiency in new larger "System-on-a-Chip" designs, design re-use needs to be an integral part of systems design flow.

Engineering Organizational Structure

Historically, engineering organizations have been designed around one of two large classes: functional organizations and project organizations (Figure 2). Most engineers and managers are familiar with the differences between these two classes. Functional organizations are built around engineering or sub-product engineering proficiencies, allowing for a focus on technology and engineering best practices. Project organizations, on the other hand, are built around a specific customer product so that engineering talent is focused on the specific needs of a customer. Both classes have their situational advantages and disadvantages.

With a larger portion of a system encapsulated in FPGA logic, there are two effects on functional engineering organizations. The first, predictably, is a higher demand for FPGA design engineers on staff, and possibly realignment in the engineering subdivisions. The second im-

Green Engineering

Powered by National Instruments

MEASURE IT

Acquire environmental data from thousands of sensors

Analyze power quality and consumption

Present measured data to adhere to regulations

FIX IT

Design and model more energy efficient machines

Prototype next-generation energy technologies

Deploy advanced controllers to optimize existing equipment

For more than 30 years, National Instruments has empowered engineers and scientists to measure, diagnose, and solve some of the world's most complex challenges. Now, through the NI graphical system design platform, engineers and scientists are using modular hardware and flexible software to not only test and measure but also fix inefficient products and processes by rapidly designing, prototyping, and deploying new machines, technologies, and methods. Today, a number of the world's most pressing issues are being addressed through green engineering applications powered by NI products.

>> Download green engineering resources at **ni.com/greenengineering** **800 890 1345**

NATIONAL INSTRUMENTS™

pact is to pull systems and architectural engineers into the FPGA design effort. This requires either a strong systems engineering capability within the hardware and firmware organization or a systems engineering staff capable of understanding the complex and new capabilities of programmable logic devices.

Project organizations are better suited for large reengineering programs to take advantage of new 40nm technologies; however they are less likely to be tracking advances in digital technology. Many times a project organization will rely on internal research and development (IRAD) or cross-project collaboration to achieve new technology insertion.

Functional organizations are more likely to be technology focused and able to translate new technologies across multiple programs. However, the momentum to adopt new chip technologies is sometimes lacking compared to that of a project organization. In both cases, some fundamental changes may be necessary in the systems engineering functions in order to take advantage of the SWaP and design efficiency advantages of design integration into larger FPGA devices.

System Design Approach Changes

How is the systems engineering process impacted when several subsystems are consolidated into larger FPGA devices and then distributed among responsible engineers?

Fundamentally, the principles of requirements engineering and test do not change. However, the lines between hardware and software can become more difficult and the concept of design interfaces expands to include data boundaries between FPGA sections (within the FPGA). This trend has existed in software engineering for some time.

Just as systems engineering now includes code and mega-executable partitioning among software IPT members, it also now encompasses FPGA architecture and design. FPGA component selection, when using larger FPGA devices, will be driven much more by system requirements than hardware requirements.

Skills Needed for FPGA Design

One of the most difficult skill sets to gain in design organizations today is "'FPGA design," where the job descriptions include:

- Strong VHDL and Verilog design experience
- Embedded computing experience
- Digital test and debug (logic analyzer) experience
- DMA and memory interface experience
- Knowledge of Ethernet over SONET, 10 GbE, SRIO, PCIe, and so on.

How many of these skills are really necessary to develop FPGA designs? The answer of course is all of them, but these skills can now be distributed among a team rather than consolidated into one or a small number of FPGA-knowledgeable design staff. As in software engineering, new skills are needed in FPGA architecture and design partitioning. These are systems engineering functions and should require only a subset of FPGA design engineering skills.

One increasingly discussed trend in both commercial and defense electronics is design outsourcing for FPGA logic devices. This allows defense sector companies to focus on core competencies and shift risk to outside engineering houses on important issues such as signal integrity on high-speed interfaces. Even where this makes sense in some engineering design organizations, it does not negate the need for strong systems level knowledge of FPGA capabilities, design partitioning and system-on-programmable-chip architecture development that will make up the most important engineering decisions in an electronic system.

Training is a difficult subject in high-technology defense companies. This is particularly true in project-based organizations, where training is an "off-the-grid" activity. The "half-life" of technical

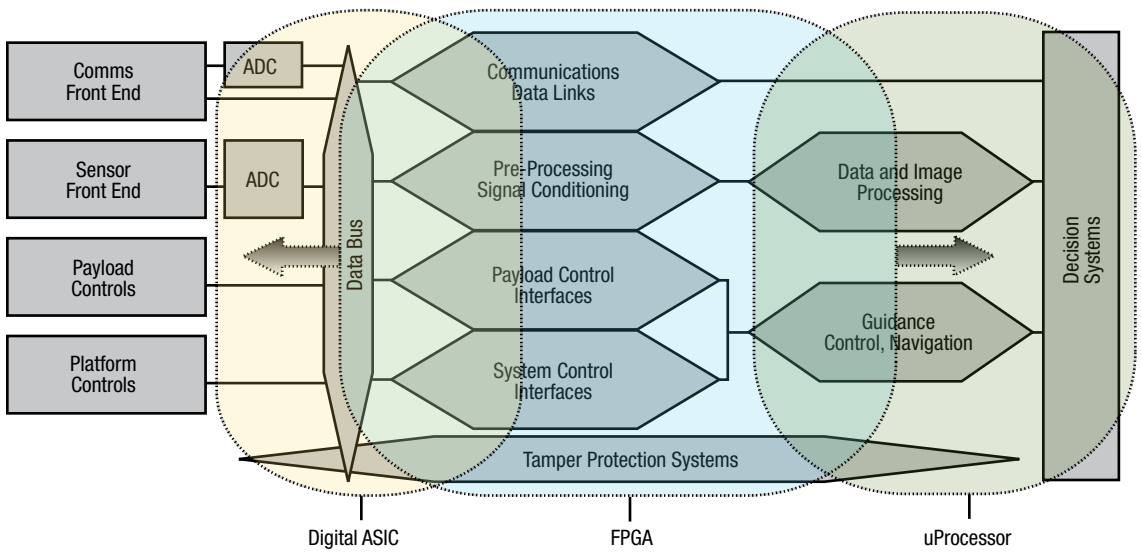


Figure 1

FPGAs are expanding in technology domain applications in military electronics.

training can be very short—sometimes less than the time needed to assess training program effectiveness. Some technical professionals claim that over half of what an engineering graduate learns in college is obsolete within five years.

It is less and less likely that engineering departments will be able to directly hire exactly the FPGA design skills they need, especially when new devices have ASIC-level complexity and require team-based design. Application level knowledge (signal processing, imaging, etc.) combined with the required FPGA design skills is even less likely.

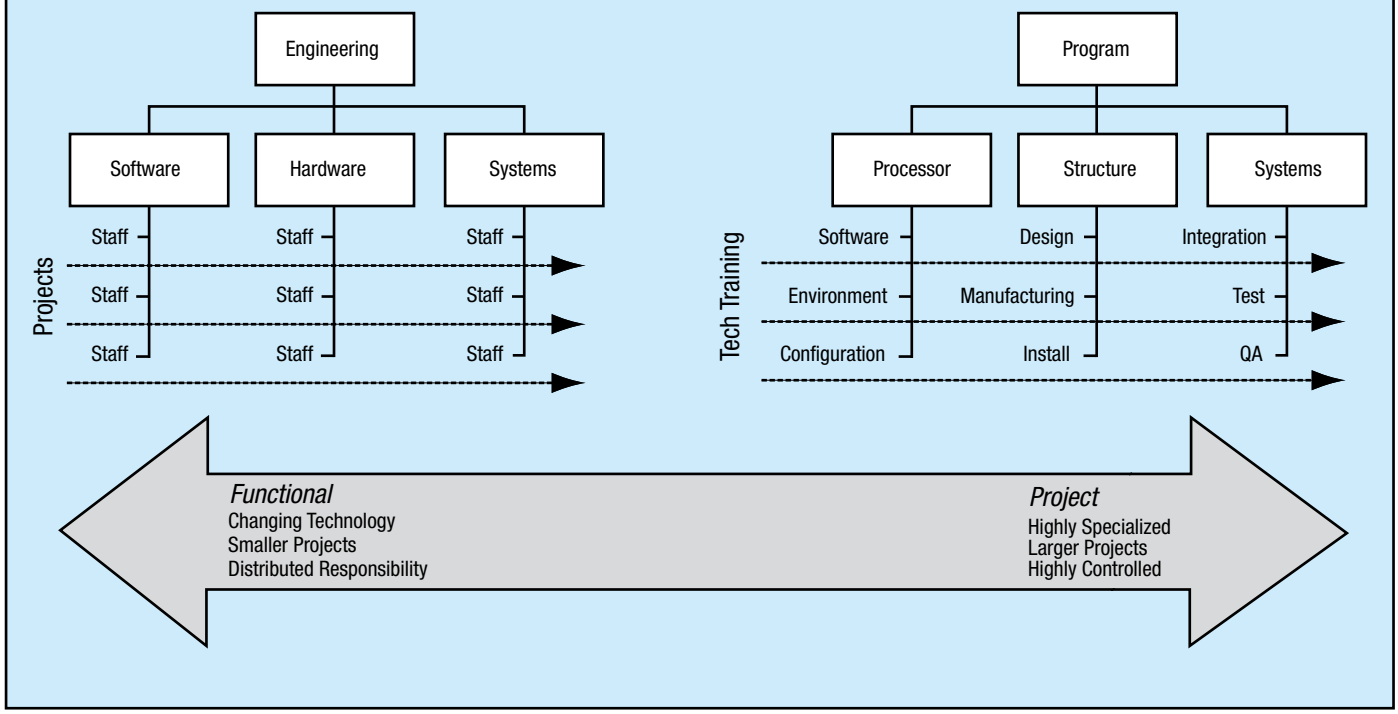


Figure 2

This diagram shows the spectrum of defense system engineering organizations, from functional to project.

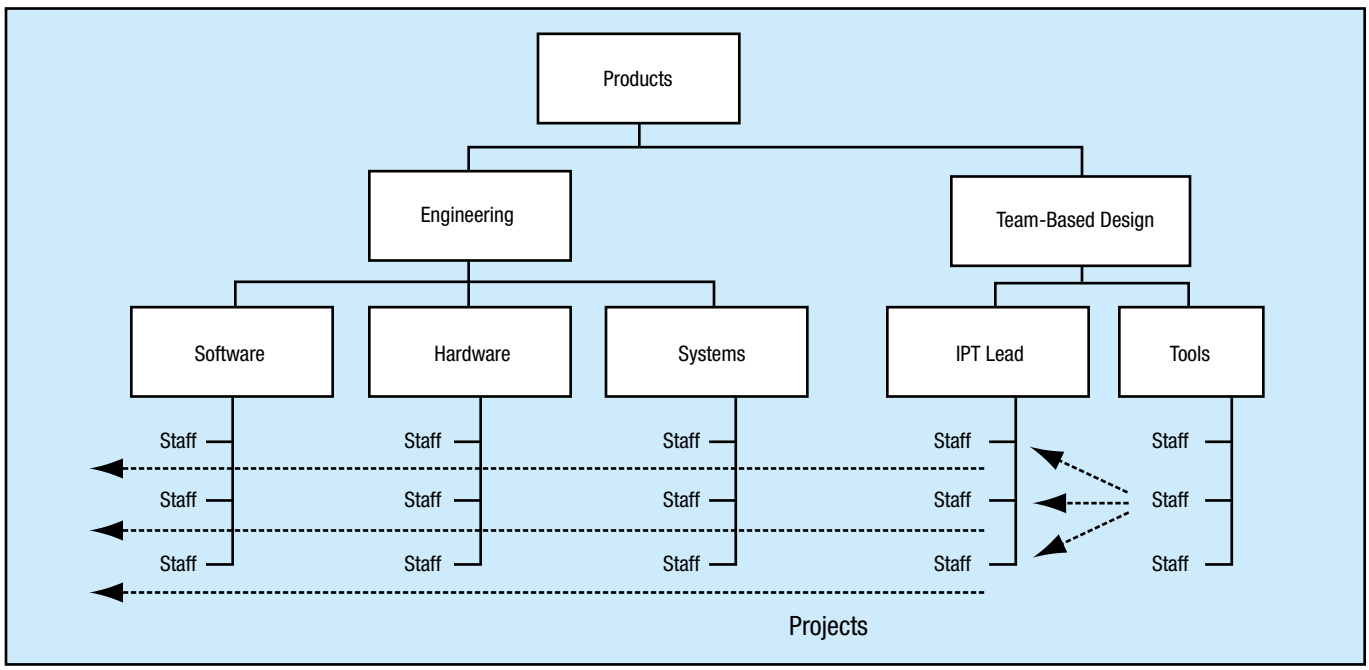


Figure 3

This engineering product organization emphases team-based design for military system development.

These difficulties can best be addressed by allowing experienced systems engineers to participate in FPGA design by using new tools with usable abstraction layers. While many processing card developers offer abstracted "development kit" solutions for application markets, these development kits will become less applicable to the wide range of user applications with the introduction of new programmable logic devices. Commonality in design entry must come from another source.

This source is FPGA vendor-developed systems tools. Virtually all FPGA vendors are developing or co-developing system design tools to meet the demands of highly integrated systems. More importantly, they are working to make their existing timing, design entry and physical synthesis tools perform more efficiently in a team-based design setting.

Defense engineering departments will continue to rely on universities, FPGA vendor-supplied training, or hiring for the FPGA-specific skills they need. It is not likely that internal training for PLD-specific skills will be cost-effective. However, it will be increasingly important to develop a company-internal team-based design process with requisite training. This process should highlight the company-approved tool flows, requirements/test/verification processes and risk management procedures. By participating in a company developed team-based design training process, design engineers will be able to more easily focus on which additional vendor training they need in order to fully participate in their design programs.

Redefining Systems Engineering

Moving up the silicon manufacturing technology curve may not seem like a good reason for reorganization. However, the reason to move to larger devices should be based on integration efficiencies and design productivity, which may necessitate changes in design roles.

The systems engineering roles in defense systems companies have evolved over the years in many ways. Among the changes in scope are the inclusion of lifecycle management, design-for-cost and manufacturability, system of systems design, and open standards architectures (to include IP reuse). These are all derivatives of a team-based design methodology aimed at generating efficiencies elsewhere in the design lifecycle.

Cost drivers in defense electronics design—architecture, partitioning, verification and board integration—are more strongly tied to design tool flow than ever before. With the potential for different vendors in each portion of the design flow, there is a great deal of risk to be managed by the engineering organization.

The fundamental structure of an organization should enable it to fundamentally manage tool flow risk, as well as the IP reuse throughout the organization. While there are many possible ways to tailor this to defense company organizations, advocating a team-based design function controlled by a systems group or IP management staff is the most effective and efficient.

In the example shown in Figure 3, team-based design and tool flow are emphasized placing all IPT managers within that organization. The primary function of the IPT lead is to pursue a systems de-

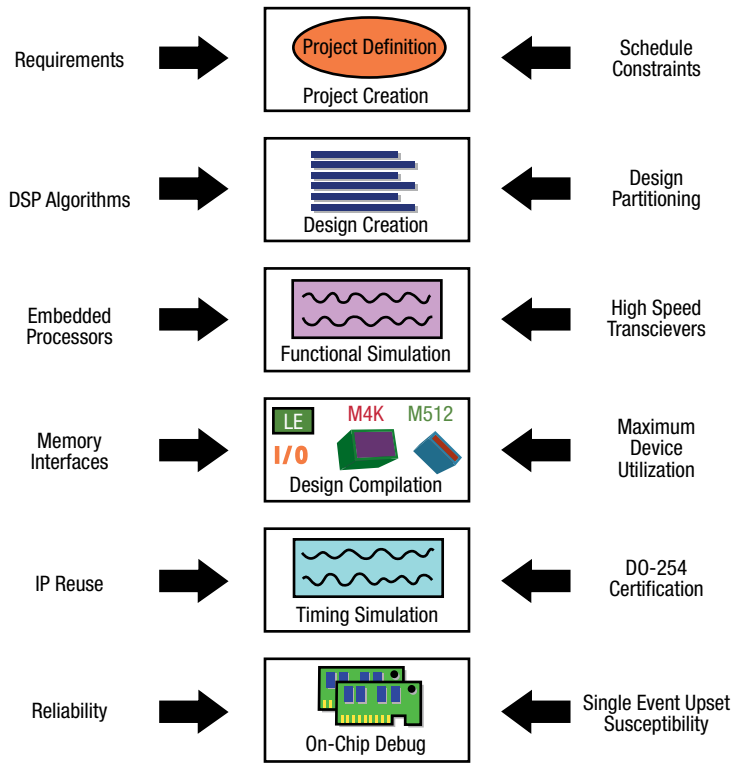


Figure 4

This illustrates the many input decisions that go into a team-based design tool flow.

sign using the best possible architecture given the current technology in tools and team-based design.

Most Efficient Design Process

Creating a functional engineering organization should take into account three primary groups: company shareholders, customers and employees. This means functional roles and skill divisions are articulated for both the best customer product and the most efficient design process for shareholders. Just as important, however, is how the new organization establishes career paths and career development for the engineers that make up the organization. Because design flow methodology is such a critical technology and a cost driver for organizations that rely on PLD design, talent and project management potentials should be driven toward these competencies as (one) path for career advancement.

While there are many temptations to focus on the newest high-density and high-speed transceiver capabilities of the 40nm generation of FPGA devices, military customers will necessarily want to focus their efforts on the impact of design flow technology in their organizations (Figure 4).

Trade studies for device selection are traditionally cost versus performance. As FPGAs become more capable of containing enough of an electronic system's functions, the number one systems cost driver is tool flow efficiency. While this is not simple to assess or measure, selecting the right tool flow for defense electronics design is paramount for cost competitiveness and efficient organizational operation. ▮▮

Altera
San Jose, CA.
(408) 544-7000.
[www.altera.com].

Fabric Test for Mil/Aero Systems: The Cost-Effective Way

Switched fabrics enable impressive throughputs in VPX and VXS. But the reality of that performance falls short unless each serial link is optimized. SerDes test blades ease the way.

Mohamed Hafed, Ph.D.
Chief Technology Officer, DFT Microsystems
Justin Moll
Director of Marketing, Elma Electronic

VPX and VXS continue to gain acceptance among developers of military and aerospace systems. These VME follow-on architectures employ fabric schemes such as Serial RapidIO and PCI Express to provide impressive system throughput. All that said, exploiting such serial fabric technologies to their maximum potential requires careful system optimization even at the physical level. Excessive signal attenuation, for example, across backplane traces can result in suboptimal system performance. So instead of achieving the theoretical aggregate bandwidth or system throughput associated with the technology, often a much lower throughput results because of the poor error rate and the constant need to retransmit erroneous packets.

To maximize performance of VPX and VXS mil/aero systems, the behavior of each serial link in each slot in a populated backplane system needs to be optimized. Doing this calls for the use of test blades: dedicated standard plug-in high-speed serial boards. These enable the optimization of serial links from any slot and any system configuration.

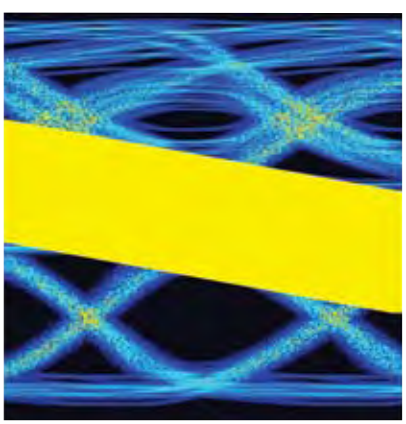


Figure 1

Eye diagrams of a serial link. In the top part of the figure, a closed "eye" is observed, whereas an open "eye" is observed in the bottom part of the figure. In general, closed eyes result in poor system bit-error-rate performance and hence poor aggregate system bandwidth.

Losses associated with variable backplane trace lengths are dependent on fabric topology. To deal with those losses, new serial transmitters can compensate by controlling parameters such as pre-emphasis and current boost. For example, a typical commercial Serial RIO device offers register control for driver strength, supply current and driver pre-emphasis. By selecting different driver settings on the device, backplane trace losses can be compensated. Figure 1 shows an example of two eye diagrams for a single serial link but with different driver pre-emphasis settings.

768 Different Driver Settings

Programmable drivers offer hundreds of settings that the system integrator can control. In fact, the typical example device mentioned above provides 768 different driver settings. With that degree of programmability, the question arises as to how a system integrator can know what driver settings to use for his or her specific system. Moreover, the amount of pre-emphasis or "boosting" is—naturally—slot dependent. The farther a slot is from the source, the more trace loss it is subjected to. In fact, no one driver setting will be applicable to all slots in a backplane. This is illustrated in Figure 2, which depicts eye diagrams obtained from a five-slot VPX chassis. A pre-emphasis setting that enables a link from slot 1 to slot 2

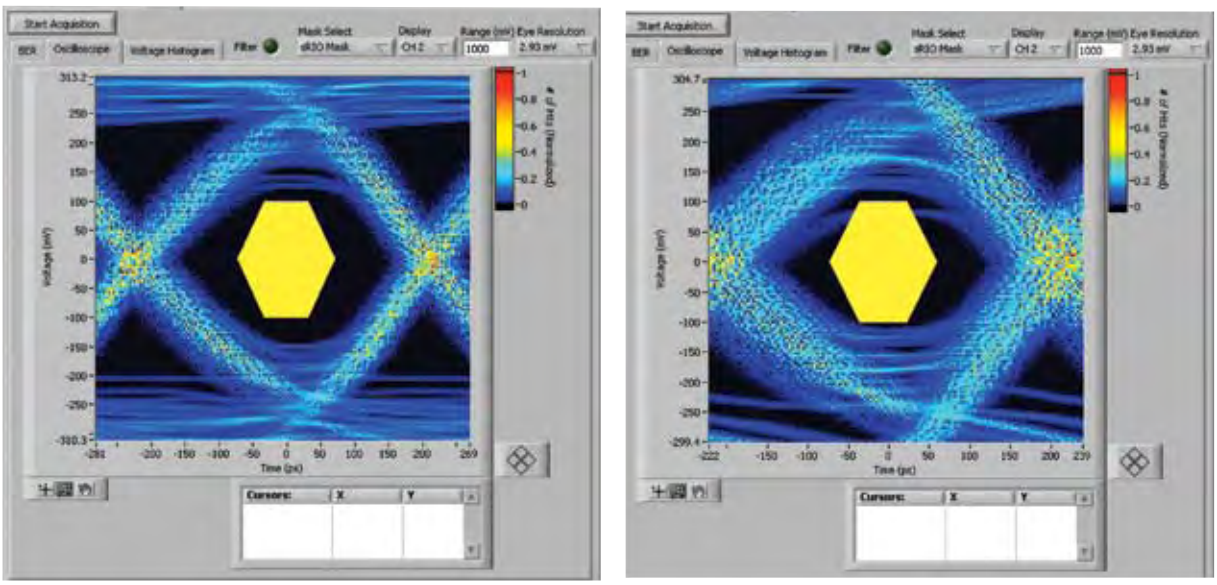


Figure 2

A single pre-emphasis setting does not work for all slot positions. For a serial link between slots 1 & 2, the setting results in a passing eye (left). For a link between slots 1 & 5, the same pre-emphasis setting results in a failing eye (right).

to pass the Serial RapidIO compliance mask is not adequate for a driver connected from slot 1 to slot 5. Clearly, a different driver setting is required for communication with slot 5 than for slot 2. When the appropriate setting is selected for the link connected to slot 5, the resulting eye diagram is as shown in Figure 3.

SerDes Test Blades

As can be seen from the above examples, there is a need for a configuration-specific tuning of transmitter pre-emphasis parameters in a system. This is where SerDes test blades, such as the DV3200 VPX SerDes Test Blade from Elma Electronic—developed in cooperation with partner DFT MicroSystems—come in. A test blade is a tool that is specifically designed to perform driver pre-emphasis tuning in a populated backplane, and it results in unprecedented productivity/efficiency gains over conventional methodologies.

Note that since VPX and VXS share the same Multi-Gig family connector, it is fairly simple to create a test blade module based on VXS. The "intelligence" of the test card is on a small module that can fit on various form factors. Figure 4 shows a schematic illustration and a photograph of a SerDes test blade that is connected to a backplane system. As can be seen, it has several important characteristics. First, it is a single-slot blade that is designed to be compliant to the target specification. For example, for the VPX standard, a test blade has a standard 6U or 3U form factor, and it connects directly to the backplane connectors in the VPX system. Second, the test blade has no external connections to test and measurement equipment. It is fully contained and is capable of performing all the functions necessary for backplane signal optimization. Third, the test blade has a USB connection to a host PC. The PC runs an easy-to-use graphcal user interface that enables access to all the test blade functions. In the next section, the use of test blades for driver pre-emphasis tuning is described.

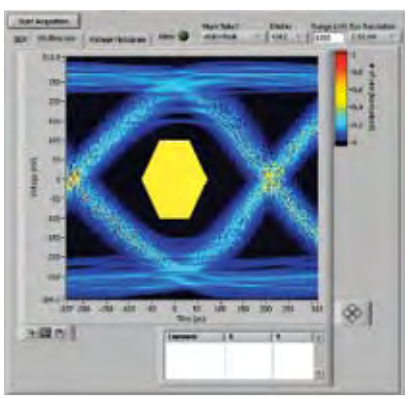


Figure 3

Adjusting the pre-emphasis setting for the link between slots 1 & 5 eventually yields a passing eye.

The driver pre-emphasis tuning process involves installing the "source"

RTD Embedded Technologies, Inc.

The Stackable PC Company™

AMD Geode™ LX 500 MHz

Intel® Pentium® M 1.4 GHz

TI 8000 MIPS dspModule™

cpuModules™
-40 to +85°C

		Intel Pentium M					Intel Celeron						AMD Geode LX	
		CMA157886PX1400HR	CMX158886PX1400HR	CMD158886PX1400HR	CMX158886PX1400HR-BRG	CMD158886PX1400HR-BRG	CME147786CX400HR	CME147786CX650HR	CML147786CX400HR	CML147786CX650HR	CMX147786CX400HR	CMX147786CX650HR	CME136686LX500HR	CME137686LX500HR
Expansion Bus	PC/104 ISA Bus	✓			✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	PCI-104 PCI Bus	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓
	PCI Bus Masters	4	4	4	4	4	4	4	4	4	4	4		4
	APIC (add'l PCI interrupts)	9	9	9	9	9	9	9	9	9	9	9		
CPU and BIOS	CPU Max Clock Rate (MHz)	1400	1400	1400	1400	1400	400	650	400	650	400	650	500	500
	L2 Cache (KB)	2048	2048	2048	2048	2048	256	256	256	256	256	256	128	128
	Intel SpeedStep Technology	✓	✓	✓	✓	✓								
	ACPI Power Mgmt	2.0	2.0	2.0	2.0	2.0	1.0	1.0	1.0	1.0	1.0	1.0		
	Max Onboard DRAM (MB)	512	1024	1024	1024	1024	512	512	512	512	512	512	512	512
	RTD Enhanced Flash BIOS	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Nonvolatile Configuration	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	RTD Quick Boot	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	USB Boot	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Peripherals	Watchdog Timer & RTC	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	ATA/IDE Disk Chip (MB)	4096	4096	4096	4096	4096	4096	4096	4096	4096	4096	4096	4096	4096
	Audio		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
	Analog Video	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA
	Digital Video	LVDS	LVDS	LVDS	LVDS	LVDS			TTL	TTL	LVDS	LVDS	LVDS	
	AT Keyboard/Utility Port	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	PS/2 Mouse	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	USB Mouse/Keyboard	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
I/O	**RS-232/422/485 Ports**	4	4	2	4	2	2	2	2	2	2	2	2	2
	USB Ports	4	2	4	2	4	2	2	2	2	2	2	2	2
	10/100Base-T Ethernet	1	1	1	1	1	1	1	1	1	1	1	2	1
	ECP Parallel Port		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	aDIO (Advanced Digital I/O)	14	18	18	36	36	18	18	18	18	18	18	18	18
	multiPort (aDIO, ECP, FDC)		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
SW	ROM-DOS Installed	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	DOS, Windows, Linux	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

visit www.rtd.com for complete product listing

dspModules™
- Coprocessors
- Accelerators

Specialty I/O
- Pulse Width Modulator
- Incremental Encoder
- Opto-isolated MOSFET

Frame Grabbers
- Single or Multi-channel
- MPEG-2 Compression

Video Controllers
- Analog VGA
- TTL and DVI panels

Communication Modules
- **Express Dual 1G Ethernet**
- Copper or Fiber Ethernet
- USB 2.0 and FireWire™
- CAN Bus & CAN Spider
- Dual Synchronous Serial
- Quad Serial w/ Ethernet
- Octal PCI Serial

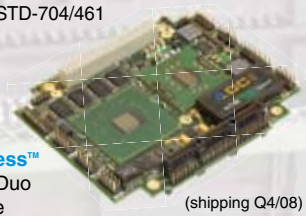
Wireless Telematics
- GSM & GSM-R
- EDGE, GPRS, SMS
- GPS & Wi-Fi

Motion Controllers
- DC Motor Controllers
- Synchro, Resolver, LVDT

Mass Storage
- 1.8/2.5" IDE & PCMCIA
- CompactFlash

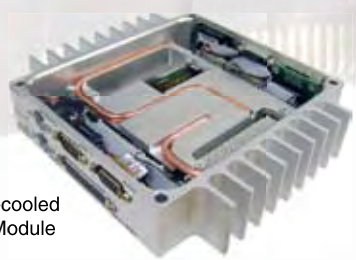
Bridge Modules
- **expressMate™**
- PCIe to PCI
- PCI to ISA

Power Supplies
- PC/104 & PCI/104-*Plus*
- **PCI/104-Express™**
- 50/75/83/88/100 Watts
- Wide input range
- ATX Power Supplies
- UPS Backup
- MIL-STD-704/461



PCI/104-Express™
Intel® Core™2 Duo
cpuModule
(shipping Q4/08)

IDAN® & IDAN*plus*™



Conduction-cooled
IDAN® cpuModule

A Founder of the PC/104 Consortium
ISO9001:2001 Certified

RTD Embedded Technologies, Inc.
103 Innovation Boulevard • State College, Pennsylvania • 16803 • U.S.A.
Phone: 814-234-8087 • Fax: 814-234-5218 • www.rtd.com • sales@rtd.com

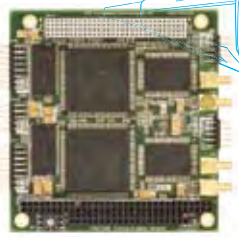
www.rtd.com

HighRel PC/104 ISA, PCI & PCIe Modules and Systems

-40 to +85°C

Autonomous SmartCal™

Wireless Telematics



Frame Grabber

dataModules® -40 to +85°C		Smart A/D		Analog I/O						Digital I/O						
		SDM7540HR	SDM8540HR	DM6420HR	DM6430HR	DM7520HR	DM7530HR	DM8530HR	DM9530HR	DM6812HR	DM6814/16HR	DM6888HR	DM7820HR	DM8820HR	DM9820HR	FPGA7800HR
Bus	Active Bus	PCI	PCI	ISA	ISA	PCI	PCI	PCI	PCIe	ISA	ISA	ISA	PCI	PCI	PCIe	PCI
	Passthrough Bus	ISA				ISA	ISA		PCI				ISA		PCI	ISA
	DMA or PCI Bus Master	✓	✓	✓	✓	✓	✓	✓	✓				✓	✓	✓	✓
	McBSP Serial Ports	✓	✓			✓	✓	✓	✓							
Analog Input	Single-Ended Inputs	16	16	16	16	16	16	16	16							
	Differential Inputs	8	8	8	8	8	8	8	8							
	Max Throughput (KHz)	1250	1250	500	100	1250	500	500	500							
	Resolution (bits)	12	12	12	16	12	16	16	16							
	Input Ranges/Gains	3/7	3/7	3/4	1/4	3/6	3/3	3/3	3/3							
	Autonomous Calibration	✓	✓													
	Data Marker Inputs	3	3	3		3										
Conversions	**Channel-Gain Table**	1K	1K	1K	1K	1K	1K	1K	1K							
	Scan/Burst/Multi-Burst	✓	✓	✓	✓	✓	✓	✓	✓							
	A/D FIFO Buffer	8K	8K	8K	8K	8K	8K	8K	8K							
	Sample Counter	✓	✓	✓	✓	✓	✓	✓	✓							
	SyncBus	✓	✓			✓	✓	✓	✓							
Digital I/O	Total Digital I/O	16	16	16	16	16	16	16	16	48	18/9	64	48	48	48	48
	Bit Programmable I/O	8	8	8	8	8	8	8	8	24	6/0		48	48	48	✓‡
	Advanced Interrupts	2	2	2	2	2	2	2	2	2			2	2	2	✓‡
	Input FIFO Buffer	8K	8K	8K	8K	8K	8K	8K	8K							
	Versatile Memory Buffer												4M	4M	4M	8MB
	Opto-Isolated Inputs											48				
	Opto-Isolated Outputs											16				
	User Timer/Counters	3	3	2	2	3	3	3	3	3	3		10	10	10	6
	External Trigger	✓	✓	✓	✓	✓	✓	✓	✓	✓			✓	✓	✓	✓‡
	Incr. Encoders/PWMs										3/9		4/8	4/8	4/8	✓‡
Analog Out	Analog Outputs	2	2	2	2	2	2	2	2							
	Max Throughput (KHz)	200	200	200	100	200	100	100	100							
	Resolution (bits)	12	12	12	16	12	16	16	16							
	Output Ranges	4	4	3	1	4	5	5	5							
	D/A FIFO Buffer	8K	8K			8K	8K	8K	8K							

visit www.rtd.com for complete product listing

‡ User-defined, realizable in FPGA

PCI/104-Express™ Analog dataModule, Dual 1G Ethernet, and Power Supply

Conduction-cooled, Hybrid RF/Embedded System

- VHF/UHF receiver
- Multi-band synthesizer
- FPGA Coprocessor
- High-end GPS receiver
- Pentium M cpuModule
- Isolated Power Supply

HiDAN*plus*™

HiDAN™ Systems

- Rugged, watertight enclosure
- Integrated tongue & groove O-ring
- Environmental sealing & EMI suppression
- Structural heat sinks & heat pipes
- Milled aluminum frames with optional heat fins
- MIL cylindrical I/O connectors
- MIL-SPEC paint & shock-mounts optional

IDAN® — Intelligent Data Acquisition Node

- Rugged PC/104 stackable framed modules
- Quick interchangeability and expansion
- Structural heat sinks, cooling fins & heat pipes
- Milled aluminum frames
- Standard PC connectors
- Optional MIL-SPEC paint & shock mounts

HiDAN*plus*™

Radar System Application

- High-end FPGA Board
- MIL Spec A/C Power Supply
- Synchro to Digital Converter
- cpuModule, relayModule and DataModules

HiDAN*plus*™ Systems

- HiDAN with IDAN modularity
- Stackable signal raceway

rtd®
"Accessing the Analog World"

"MIL Value for COTS prices"™

blade into the slot for which it is intended. The source blade is the board for which the serial driver parameters are being optimized. Meanwhile, the SerDes test blade is installed at the slot where the "destination" blade is anticipated to be placed. This is the slot at which the serial link for the "source" blade is terminated. For a slot 1 to slot 5 connection, let's say the source blade is installed in slot 1 and the test blade in slot 5. At this point, the hardware setup is complete, without requiring any external benchtop equipment.

Next come the software steps. The source blade is programmed to generate a test pattern, such as a PRBS7 pattern. Most new serial devices include test patterns such as this example. Subsequently, the SerDes test blade is programmed to lock onto the test pattern and measure signal parameters such as eye diagrams and bit-error-rate. Once this is done, a software loop is started in which the driver pre-emphasis settings are incremented sequentially and eye diagrams are collected for each driver setting. The eye diagrams are analyzed within the test blade software environment to assess compliance to a specified mask (such as Serial RapidIO). The loop terminates as soon as the eye diagram passes compliance.

At this stage, the appropriate driver pre-emphasis setting is recorded for the source blade. This setting represents the optimal setting for the source blade in the specific system configuration. Specifically, if the source blade happens to be installed in a different system, the optimization process needs to be repeated for the new system. Figure 5 shows the eye diagram optimization process graphically using real data from a 5-slot VPX chassis.

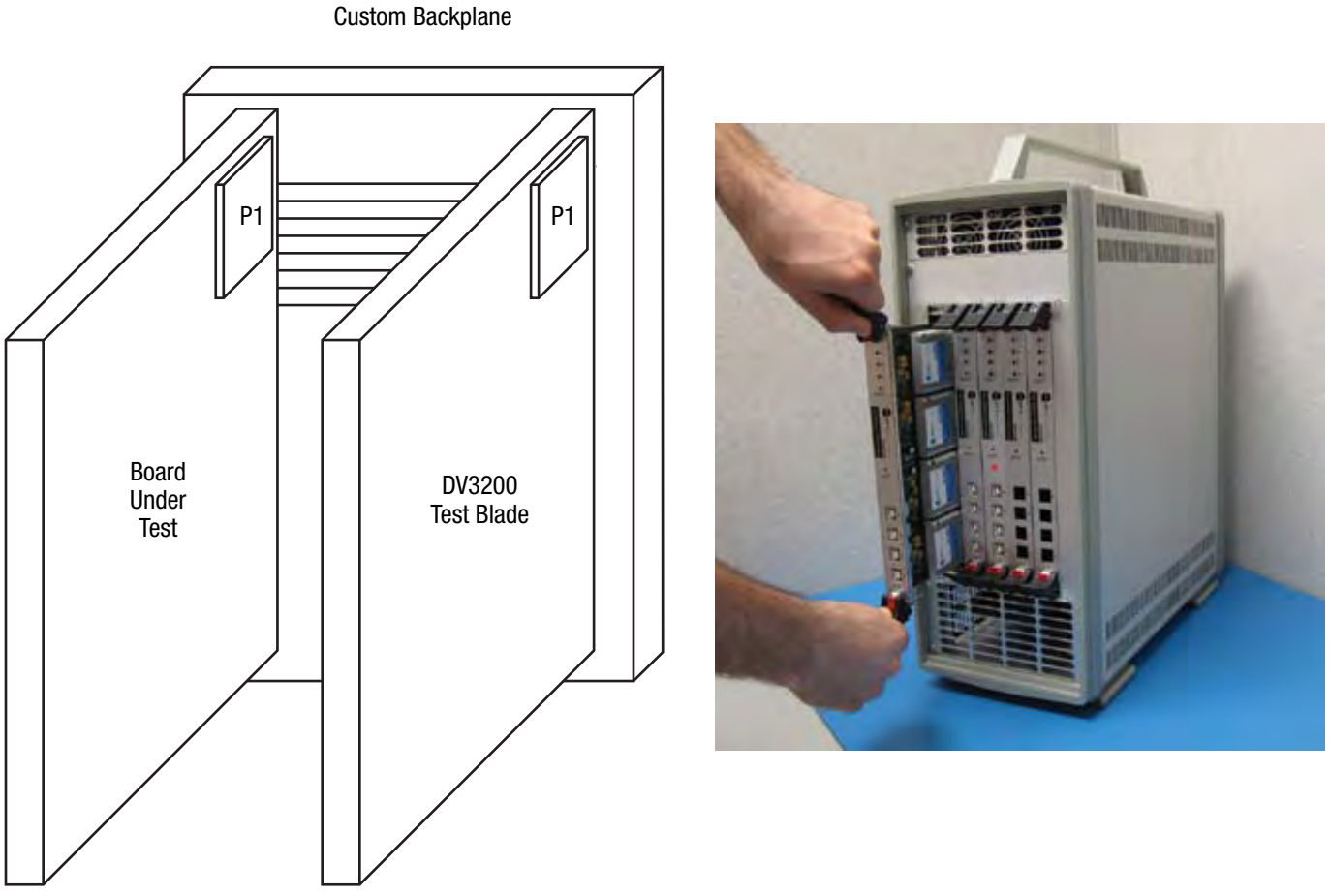


Figure 4

Illustrated here are SerDes test blades and their application in populated chassis (left), and photograph of test blade insertion into a 5-slot portable chassis (right).

True Bit-Error-Rate Optimization

SerDes test blades, such as the DV3200, offer more than just eye diagram plots as shown earlier. In fact, they provide detailed analysis functions for the complete evaluation of serial link transmitters as well as receivers. Most

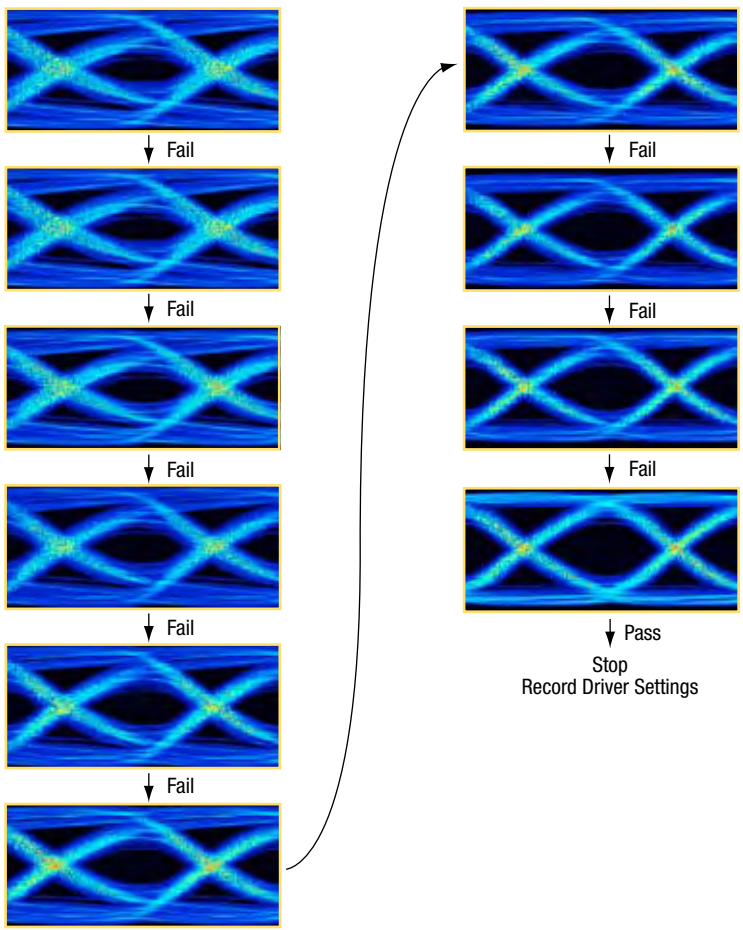


Figure 5

Pre-emphasis tuning example. Notice progressively larger eyes.

importantly, they offer the opportunity to evaluate bit-error-rate (BER) performance of systems under varying conditions (ambient conditions, software conditions, computing payload and so on). Figure 6 shows various BER contour plots that are captured using a test blade. Contour plots are useful utilities to evaluate the amount of margin in serial links.

SerDes test blades represent a truly compelling productivity enhancement solution for VPX and VXS users in the military and aerospace industry. All that is required to operate a test blade is a PC with the appropriate software loaded, USB cables and one or more test blades. This approach enables system-level optimization to occur simply and with great efficiency. ■■

DFT Microsystems
Montreal, Quebec
Canada.
(514) 878-8271.
[www.dftmicrosystems.ca].

Elma Electronic
Fremont, CA.
(510) 656-3400.
[www.elma.com].

System Development

New Approaches to Military Test

Enhanced HALT Techniques Boost MTBF Prediction

By improving HALT processes it's possible to provide accurate product life values. The gathered knowledge helps military system designers build rugged, reliable electronics for harsh environments.

John E. Starr, Consultant
CirVibe

There's a commonly accepted notion that HALT and repetitive shock (RS) vibration cannot provide mean-time-between-failure (MTBF) values for electronics. Military and aerospace electronics systems are often too expensive to allow an adequate sample size for statistical predictions (required for MTBF). Moreover, HALT chambers typically lack accurate control of vibration excitation in frequency ranges critical to circuit card assembly (CCA) failures. This makes it a challenge to obtain a numerical definition of damage excitation.

Major advanced military programs like Future Combat Systems (FCS) and Joint Strike Fighter (JSF) (Figure 1), for example, are striving to reduce maintenance costs through high-reliability requirements and application of prognostics for the programs' electronic systems. HALT (highly accelerated life testing) is not intended to simulate an actual field environment. Its intent is to stimulate natural responses that will find assembly weaknesses. By finding product weaknesses, understanding causes of failure and redesigning to obtain a more rugged product, product ruggedness and reliability can be increased. MTBF is not an important number if product life capability greatly exceeds design requirements—if product life capability is known. The term "greatly" is used because the distribution of failure of electronics under vibration is wide and, with limited testing, not often well defined. For effective HALT, understanding failures and understanding the improved product are critical to reliability improvement.

Frequently, when the military asks suppliers to improve electronics due to

Figure 1

Major advanced military programs like Joint Strike Fighter (JSF) are striving to reduce maintenance costs through high-reliability requirements and application of prognostics for the programs' electronic systems. HALT's intent is to stimulate natural responses that will find assembly weaknesses. Shown here, a new F-35 Lightning II Joint Strike Fighter makes its initial flight over Fort Worth, Texas.

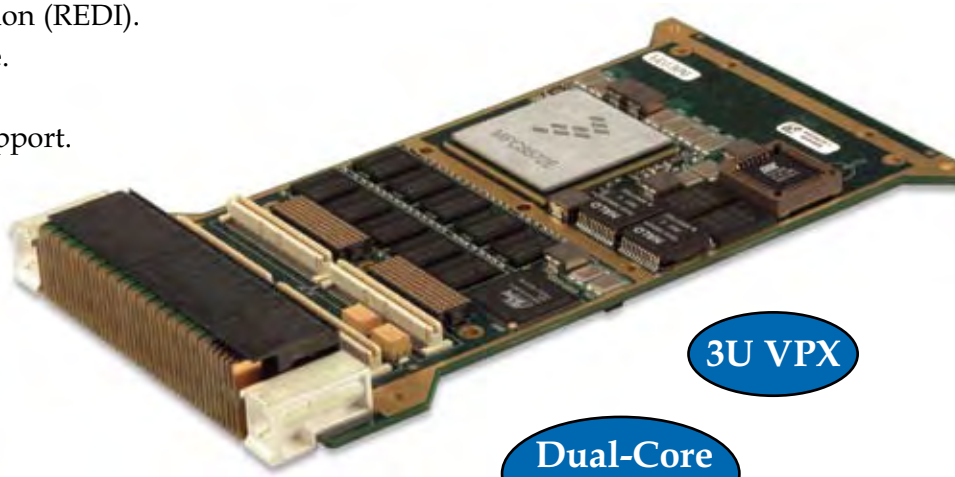
Some Things Just Can't Be Ruggedized...

...And Some Are Designed Rugged From Day One

Bringing the Freescale MPC8572E to VPX, Extreme Engineering Solutions introduces the **XPedite5370**, a high-performance 3U VPX-REDI single-board computer. With the Freescale MPC8572E dual-core PowerPC processor, the **XPedite5370** offers:

- Dual-Core Freescale MPC8572E processor at up to 1.5GHz.
- Two independent DDR2 SDRAM channels for maximum bandwidth.
- PCI Express and SERDES Gigabit Ethernet P1.
- Ruggedized Enhanced Design Implementation (REDI).
- XMC and Processor PMC (PrPMC) interface.
- 3U VPX-REDI conduction or air cooling.
- Linux, VxWorks, QNX, and INTEGRITY support.

NEW!



3U VPX

Dual-Core PowerPC

For customers looking for one vendor to provide the complete system solution, X-ES provides full component selection, operating system support and integration services.

X-ES

Extreme Engineering Solutions

www.xes-inc.com 608-833-1155 sales@xes-inc.com

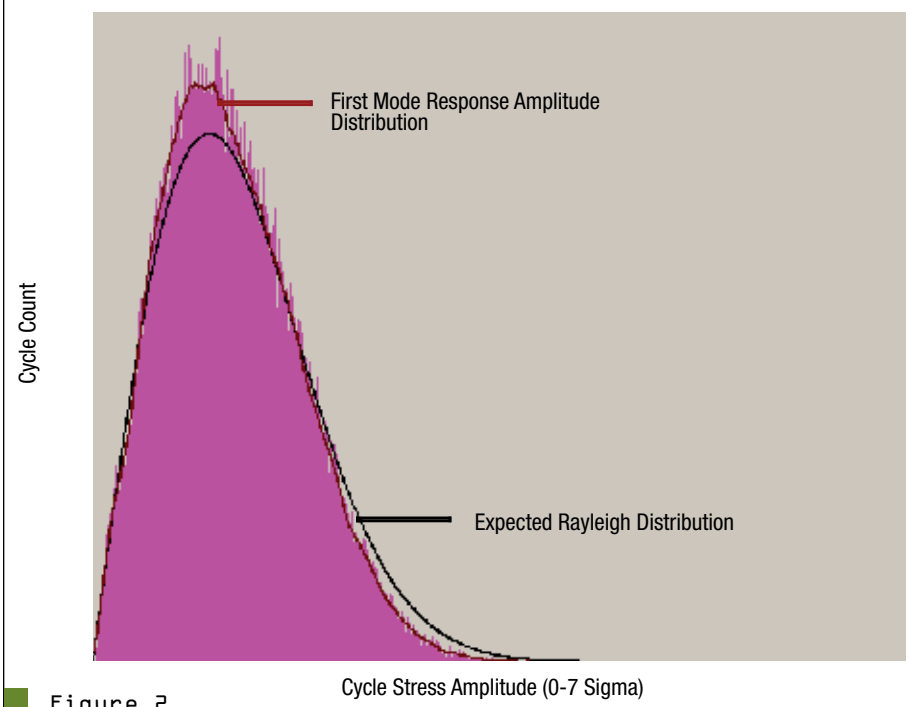


Figure 2

Shown here is the ED Shaker circuit card assembly First Mode Response Amplitude Distribution. The ED Shaker circuit card response closely matches the expected Rayleigh response.

shortfalls in reliability, the redesigned product has even lower reliability. Electronic assemblies are very complex. Testing performed without an in-depth understanding of the product and the test equipment can give misleading results.

As an example, HALT vibration excitation is quasi random. The chamber cannot impose a continuous flat vibration spectrum. It can excite some natural frequencies of an electronic assembly at much higher levels than others. When comparative HALT is performed—a process where two different products are tested to find fragility levels—one might conclude that a product that failed in HALT at 35 g's is more rugged than another product that failed at 25 g's. This can be the wrong conclusion. The real answer can be found in how much damage each HALT vibration test imposed relative to the expected damage exposure in the service life environment.

Consider a service life vibration environment that has characteristics of a continuous flat spectrum and chamber excitation that is isolated from the 35 g product weakness but coupled well to the 25 g product. The 35 g product may fail at higher g levels, not because it is more rugged, but because "frequency separation" protects its weakness from chamber vibration. The 35 g product might be far less reliable in service life. Understanding both product and test will avoid judgment error.

Service Life Vibration

The assumption that HALT cannot provide definable product life values is true only if technology advancements of the past decade and a half are ignored. Vibration damages the product using some fraction of the available service life. Quantifying response can relate vibration exposure to life use. Equivalent service life vibration has historically been performed on ElectroDynamic (ED) shakers because they are capable of providing relatively well-defined and consistent vibration excitation. The expected distribution of natural frequency response peaks of the product on an ED shaker is represented by the Rayleigh Distribution. Figure 2 shows the distribution of measured peak CCA responses from an actual test of an electronics assembly on an ED shaker as well as a perfect Rayleigh distribution. Life predictions have historically been made by calculation of damage assuming a perfect random response distribution of peaks of first mode response.

Exponential advancements in computer power since the introduction of HALT have greatly expanded both test measurement and fatigue damage analysis capabilities. These advancements have made detailed evaluation of life-use (fatigue damage) possible under any excitation type: HALT chamber or ED shaker or other.

Measuring Responses

Even when the excitation profile cannot be controlled, response can be measured. Test measurements allow accurate response cycle count. Figure 3 shows first mode response cycle count data (same CCA as in Figure 2 test) from a HALT chamber, showing cycle count plots for two locations within the chamber. The distributions of responses, performed under identical vibration control settings, have different shapes and different peak amplitudes. There are very large differences in damage accumulation for the two locations. Even with differences, the CCA damage at each location can be determined.

Advancements in computer power provide the ability to analyze stresses in CCAs in great detail, understanding how each critical vibration mode contributes to fatigue stress cycles. With the ability to accurately analyze detailed stresses, damage to failure can be determined for any response distribution, which in turn can be extrapolated to time-to-failure for any other response distribution (including field service life loads).

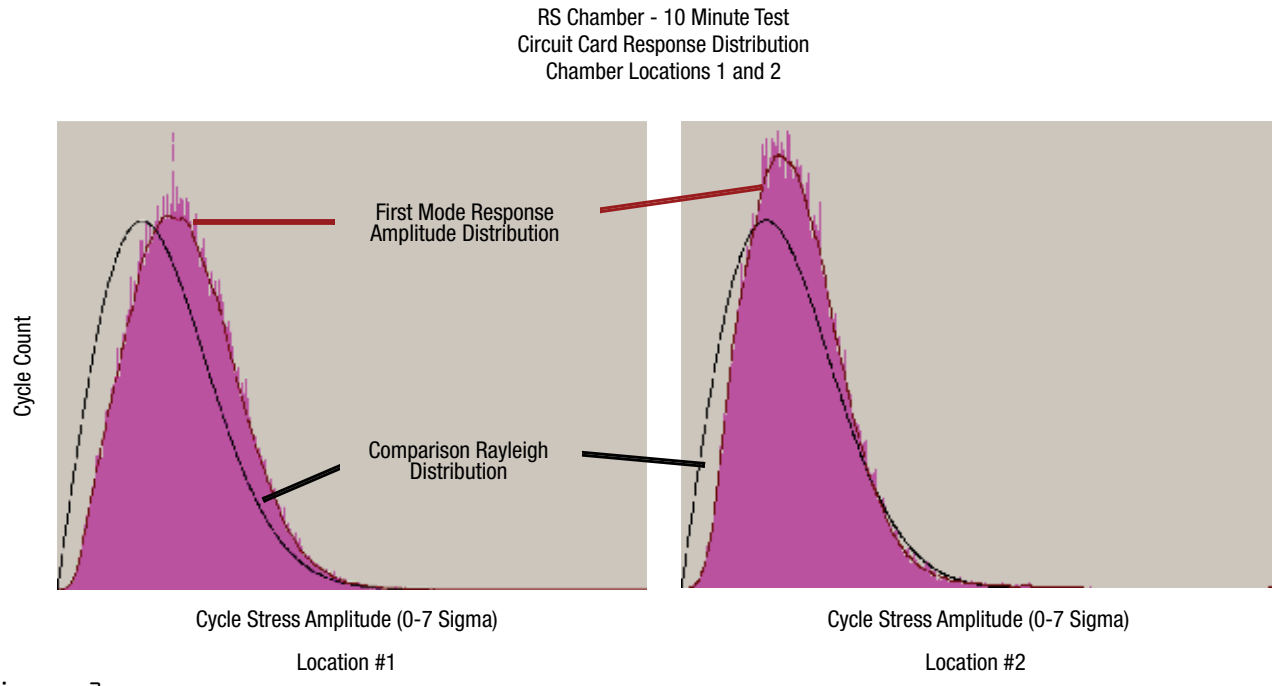


Figure 3

Shown here is the RS Chamber circuit card assembly First Mode Response Amplitude Distribution. The response distribution, critical to damage control, varies significantly with test position

For decades, electronics vibration life has been understood through the combination of analysis and test. Product reliability has required unique development testing for each product or product revision without the benefit of past experience. For vibration, even two CCAs with identical parts but different layouts can differ in MTBF by many orders of magnitude. Identical components in different positions or different assemblies do not have different life capabilities because they are stronger or weaker in different locations. They have different life capabilities because they experience different damage accumulation rates.

Empirical Equations Fall Short

Due to the complexity of CCAs and the high cost of computer analysis over much of the history of HALT, empirical equations have been commonly used for life predictions. Of course, a single equation is not capable of describing all the complexity of stress flow within an electronics assembly with multimode vibration response. In-depth product understanding cannot be developed with that combination of test and analysis (one equation fits all).

Determining Failure

Accuracy of the numerical definition of failure is dependent on the vibration control levels and the accuracy of applied analysis. Vibration equipment—HALT chambers or even ED shakers—do not create perfect Rayleigh response—the first contribution to life prediction error. Additional error occurs by application of an oversimplified analysis.

The advancements in computer technology now allow any company involved in development or production of electronics to have a higher level of analysis and test. Product understanding to the level of knowing which solder joint is at the highest risk of failure can now be obtained with a PC-level of fatigue analysis. CirVibe has developed purpose-built vibration life software that performs detailed component-level fatigue damage analysis for electronics performed on a PC. This analysis includes detailed stresses, both flexural and inertial for CCA multimode response. The analysis model creation is highly automated so the user does not need finite element expertise. Analysis calculates detailed stresses using millions of equations.

Under random vibration, all vibration modes are excited simultaneously. Each response cycle in each mode creates stress distributions in all components. Due to the exponential relationship between cycled stress and life, the combination of stresses causes failures to occur at higher rates than rates that would occur if only one mode was responding. For most CCAs, the assembly fragility is dominated by response within the first 3 modes—usually the first.

Special Cases, Modal Responses

Special cases might have components that fail due to their own modal response, but this is not common for SMT and also not usually resolved by major product redesign, but resolved through local modifications. How much faster a component fails due to the multimode stress condi-

tion depends on the magnitude of stress contributions from all modes. Detailed analysis can determine which modes should be measured during tests. Response cycle count can be performed for each critical contributing mode.

Application of detailed analysis increases the value of test. CirVibe can extrapolate component life data across assembly position or design configurations. The ability to extrapolate data across designs makes statistical analysis approaches efficient. Otherwise, every design development would rely on testing performed on that product alone without benefit from previous experience.

Historically, the ED shaker testing and calculation of expected failure time under the expected field service environment has included only first mode damage. The advancements discussed above improve on methods used with well controlled vibration equipment (ED Shaker), but also greatly expand capabilities of HALT chambers.

The greatest obstruction to development of expensive military and aerospace electronics product understanding is the limited samples of items available for test. Understanding can be maximized with numerical definition of failure. Electronic product vibration understanding is cumulative. Since numerical definition of failure is transferable across design configurations, each test benefits from the knowledge gained in previous tests that had failures of similar components. Ruggedness and reliability of electronic products occur through in-depth understanding of the product and understanding of the test.

Upgrading Reliability Design Methods

HALT can be upgraded to provide valuable product life values. For expensive hardware, every vibration test performed with life-use analysis adds information critical to product understanding. If life-use data is in the proper form, data extrapolates across design configurations. Accumulation of knowledge contributes to the growth in ability to produce rugged, reliable electronics for harsh environments. Product improvement and product life comparisons—as in redesign or comparative HALT—can be made with greater understanding and therefore less risk.

These same cycle count plus analysis methods can be used for more accurate determination of life expectations for ALT (Accelerated Life Tests) performed on ED shakers. The methods can also improve decisions on HASS and ESS (Environmental Stress Screening—ED Shaker) testing of electronics for obtaining higher reliability. When products are understood at the component level, reliable and rugged products result. ▮▮

CirVibe
Plymouth, MN.
(763) 559-5166.
[www.CirVibe.com].

Keep Your Design...

Change Your Perspective.

It takes creative thinking to launch breakthrough solutions. Whether we optimize board space, work with environmental extremes or solve component incompatibilities, be assured that your design can be realized with our advanced microelectronics solutions. See your great ideas take flight at www.whiteedc.com/design.

602.437.1520 TEL | 602.437.9120 FAX

WHITE ELECTRONIC DESIGNS

www.whiteedc.com

Customer First. Quality Always.

Technology Focus

Rugged Displays

Rugged Displays Climb the Resolution and Reliability Curves

With demand increasing in the military for advanced graphics and video, display technology is bringing high-resolution, high-performance displays into mainstream use.

Jeff Child
Editor-in-Chief

High-performance display systems—large and small—have become a critical part of military operations and training. As the U.S. Military moves toward network-centric operations, demand will rise for electronic systems that provide data communications. All the many end-nodes of a networked military—tanks, aircraft, ships and man-portable gear—will need to process and display all that data shared among the nodes. Feeding those needs, makers of embedded graphics boards are leveraging advanced graphics processing technology, often using silicon targeted for the gaming market.

An example of this new breed of display subsystems is Gables Engineering's new, reconfigurable, Multi-Function Display (MFD) system targeted at aircraft flight deck applications. Gables Engineering selected Quantum3D IGL178 and IData178 to use this reconfigurable, MFD system. IGL178 (Figure 1) is a software-based Graphics Processing Unit (GPU) for FAA DO-178B Level-A-certifiable OpenGL Safety Critical (SC) and OpenGL Embedded Systems (ES)-based applications, and IData178 is the avionics industry's leading FAA DO-178B Level-A-certifiable model-based Human Machine Interface (HMI) and embedded visual computing application development and deployment software tool suite.

Developed by both companies in close cooperation, the Gables Reconfigurable MFD includes smart display technology that enables the system to support important flight deck functions including Attitude Direction Indicators (ADIs), Horizontal Situation Indicators (HSIs), soft controllers and other capabilities on a reconfigurable platform with significantly reduced FAA or other authority safety-critical certification expenses.

Exemplifying the Navy's drive toward higher performance displays, the U.S. Navy selected Barco Federal Systems (BFS) to provide rugged display technology for the Navy's Common Display System (CDS) Remote Displays program. BFS was selected by prime contractor DRS C3 Systems. Both companies will collaborate to develop 40-inch and 65-inch Remote Displays to be used for collaborative decision making inside the Combat Information Center rooms and ship bridges and other spaces within the U.S. Navy DDG-1000 platform (Figure 2).

With the CDS Remote Displays program, the U.S. Navy establishes a family of displays that can be implemented on virtually any Navy surface ship, providing a common interface to the Navy's Platform Open Architecture Computing Environment. Remote displays are network-based rugged displays that are used to provide collaborative viewing at differ-

Figure 1

Quantum3D's IGL178 is a software-based Graphics Processing Unit (GPU) for FAA DO-178B Level-A-certifiable OpenGL Safety Critical (SC) and OpenGL Embedded Systems (ES)-based applications.

ent locations of the platform, facilitating decentralized decision making. CDS systems have an intended service life of 30 years. The DRS/Barco team will develop 40-inch and 65-inch rugged displays with integrated computing modules, which will perform local processing as needed. Each display can be mounted on nearly any shipboard bulkhead location and will accept analog, digital and internet protocol signals, with multiple inputs for each.

Night Vision Display Challenges

On the aircraft display side, there are particular challenges such as night vision. In March, White Electronic Designs Corporation (WEDC) was selected to design and manufacture a Night Vision Imaging System (NVIS) integrated panel for a government aircraft application. The project employs WEDC's Electromechanical Products Divisions' knowledge of military aircraft assemblies, expert design and build-to-print capabilities for the integrated NVIS control panel. One of the major requirements of the project was to ensure the cockpit illumination did not emit energy that could interfere with infrared-sensitive night vision goggles or other night vision equipment. The night vision goggles used in military aircraft are responsive to low light level intensities and employ high gain electronic image intensifiers that are sensitive to light in the near-infrared and infrared regions.

The infrared emissions from the cockpit illumination must be removed or eliminated to a degree that there is no interference with the use of the night vision equipment while providing sufficient brightness for direct viewing with the unaided adapted eye. The WEDC-designed NVIS control panel will also minimize the emissions in the infrared region without affecting the portion of the visible spectrum to which the human eye is most sensitive.

At last month's Society of Information Display (SID) show, a number of vendors rolled out new rugged display products. Among these were Edge Electronics EDOPH-115-NDV display—a high bright, completely enclosed, metalized LCD monitor developed specifically for integration into custom cabinets and control panels. This family of industrial-grade sheet metal enclosed displays is designed to easily embed into a host of military subsystems. This LCD display is a 15-inch TFT active matrix panel measuring 304.1 x 228.1 mm, with pixel pitch of 0.297 x 0.297 mm. Maximum resolution is 1024x768 and contrast ratio is 350:1, with a brightness rating of 1800 cd/m².

The EDOPH-115 display is driven by Digital View's HE-1600 LCD controller (Figure 3), one of DV's family of HE Series ruggedized controllers. The HE controllers are designed specifically to aid manufacturers building hardened military and industrial LCD display systems. The HE-1600 features wide-tolerance

The Many Dimensions of Display Ruggedization

Active matrix liquid crystal displays (AMLCD) that integrate environmental protection, sunlight readability and enhanced visual definition are some of the base requirements in defense and aerospace applications. These same requirements are quickly becoming the fundamental cornerstones for successful and high-efficiency commercial display applications. Because of the convergence of these market landscapes, defense and aerospace designers now have a choice between specifying a display that is custom designed to meet full defense ruggedization specifications, or choosing a commercial display that can be ruggedized to meet almost all of the military environmental specs, driving how displays are integrated into ruggedized military and aerospace applications.

As high-volume, commercial display manufacturers improve performance and expand production capacity, they are increasingly turning to non-laptop markets for areas of growth. Many of the requirements of these consumer, industrial, medical, transportation and commercial markets have similarities to the needs of military and aerospace display users, but do not fully encompass the full dimensions of display ruggedization for defense and aerospace applications. Each defense/aerospace application will have its own dimension of ruggedization.

The ruggedization process must accommodate temperature extremes, both operating and storage, over repeated cycles, extreme vibration and shock levels and high altitude while the optical processes must minimize front surface and inner structure reflections while optimizing contrast and color saturation. Over time, even the best gasket can wear and crack. If this happens in an environment that is dusty or dirty, foreign particles can work their way into the air gap between the protective window and the polarizer of the LCD.

One display enhancement that can effectively address all dimensions of ruggedization is glass lamination. Glass lamination, also known as optical bonding, is a means of optimizing the contrast in high ambient light conditions while at the same time protecting the AMLCD from the environment by filling the air gap that can accumulate moisture and other visible contaminants.

Max-Vu is White Electronic Designs' proprietary optical bonding process that attaches an optically matched filter (glass or synthetic) to the front of the display with an optically matched adhesive. This reduces internal reflections and ensures that the gap between the display and filter cannot degrade due to fogging, or the accumulation of dust. This process ensures that the image leaving the display will exit the front filter with the minimum loss and much higher contrast ratio throughout the product's lifetime. Additional benefits of the Max-Vu optical bonding process are improved robustness and impact resistance, and a very fast production cycle time.

—White Electronic Designs. Phoenix, AZ.. (602) 437-1520. [www.whiteedc.com].

Figure 2

The DDG 1000 is the lead ship in the Zumwalt class of next-generation, multi-mission surface combatants tailored for land attack and littoral dominance with capabilities designed to defeat current and projected threats as well as improve battle force defense. The ship's network is called the Total Ship Computing Environment Infrastructure (TSCEI), and it implements the U.S. Navy's open architecture strategy.

The Zumwalt-class ships rely on automation and networking to reduce the manpower that operates and supports the ship. The reduction is planned at 50% of the crew that is currently manning U.S. naval destroyers. Each ship has two 10 Gbit Ethernet backbones, with Ethernet switches to bridge the backbone to 1 Gbit Ethernet interfaces. Two ships are currently being built by separate contractors, with the potential for a joint effort to build a third. Eight ships are currently scheduled to be built.

power supplies (±25%), low mass tantalum capacitors for maximum vibration and shock tolerance, conformal coating, laboratory certified operating temperature range from -40° to +80°C, and calculated MTBF in excess of 150K hours.

Advances in Multiple View Displays

At the other end of the display size spectrum, RGB Spectrum this month introduced its QuadView HD, a new type of intelligent display processor for applications requiring the display of multiple images on a single monitor or projector. RGB Spectrum introduced the first QuadView multiviewer in the industry almost ten years ago. The concept of displaying four graphics and video signals simultaneously on a video screen has won significant traction in the industry. The QuadView HD accepts high-resolution DVI, RGB, HDTV, S-Video, component

ACROMAG FPGA I/O SOLUTIONS

Simply Powerful. Powerfully Simple.

VIRTEX™ 5

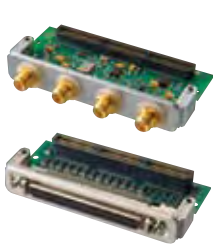
High-performance FPGA I/O designed for faster and easier development.

Only Acromag gives you a reconfigurable FPGA wrapped with just the features you need for fast and easy implementation. These PMC modules provide a high-speed I/O interface with plenty of memory for efficient data handling.

- Virtex-5 FPGAs (VLX155T/110T/85T or VSX95T) are optimized for logic or DSP
- Two banks of high speed 32M x 16-bit DDR2 SDRAM handle high volumes of data
- Two banks of 256K x 32-bit dual-port SRAM optimize DMA transfer to the bus
- PCI-X 133MHz 64-bit interface ensures fast data throughput
- Engineering Design Kit speeds development of custom FPGA applications.

Plug-in I/O cards extend the I/O capabilities

AXM I/O extension modules expand interface support for a wide variety of analog and digital I/O signals.



Affordable FPGA-based I/O for all your projects

Acromag's full line of industry pack and PMC modules feature Xilinx FPGAs at a range of price and performance points. Why settle for generic I/O when you can cost-effectively design just what you need?

For details on the fastest and easiest way to develop FPGA I/O visit

AcromagEmbedded.com, or call 1-877-295-7084

Acromag®
THE LEADER IN INDUSTRIAL I/O

acromagembedded.com • solutions@acromag.com • 877-295-7084 or 248-295-0310

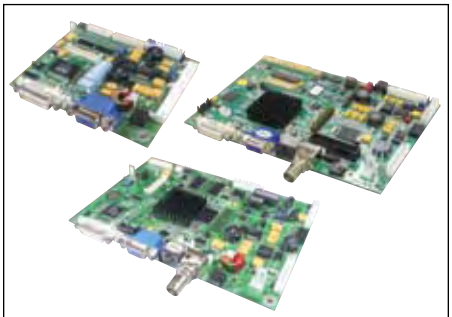


Figure 3

Digital View's HE-1600 LCD controllers are designed specifically to be part of hardened military and industrial LCD display systems. The HE-1600 features wide-tolerance power supplies, low mass tantalum capacitors for maximum vibration and shock tolerance, conformal coating, temp range from -40° to +80°C and MTBF of over 150K hours.

and NTSC/PAL composite video. Up to twenty-four sources can be connected, any four of which can be displayed simultaneously. The QuadView HD offers the highest quality graphics and HDTV rendition, with state-of-the-art deinterlacing and scaling.

An agile video switcher accepts up to sixteen video inputs, user configurable as sixteen composite, eight S-Video or five component video inputs, in any combination. Up to sixteen video inputs can be cycled through a single window with user-selected timing. The QuadView HD supports real-time, dynamic movement and resizing of windows. Each input can be scaled and positioned anywhere on the screen, as well as panned and zoomed to emphasize areas of interest. Display alternatives are virtually infinite and include quad split, side-by-side, picture-in-picture and overlapping windows. User-selectable output resolutions of up to 1920 x 1200p and up to 2048 x 1080p ensure a perfect match with any display. With DVI inputs and outputs, a completely digital signal path can be maintained from signal source to display. ▮▮

Barco Federal Systems
Duluth, GA.
(678) 475-8000.
[www.barco.com].

Digital View
Morgan Hill, CA.
(408) 782-7773.
[www.digitalview.com].

RGB Spectrum
Alameda, CA.
(510) 814-7000.
[www.rgb.com].

White Electronic Designs
Phoenix, AZ.
(602)437-1520.
[www.whiteedc.com].

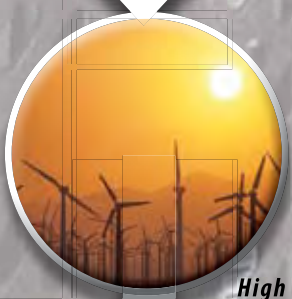
DATA STORAGE TECHNOLOGY

RPC12 Ruggedized 3U Fibre Channel RAID System

Phoenix International designs and builds rugged COTS Data Storage Systems that plug and play in any application -- from Multi-Terabyte Fibre Channel RAID and Storage Area Network configurations to plug-in Solid State Disk Drive VME/cPCI Storage Modules. We've earned a worldwide reputation for excellence by manufacturing highest quality data storage products supported by unparalleled customer service and support.

Low Operational Temperature

-20° C



High Operational Temperature

+60° C

Operational Altitude to 45,000 feet

- ***Operational altitude to 45,000 feet***
- ***Operational Temperature -20° to +60°C***
- ***Redundant, hot swap components/FRU's***
- ***40Hz to 440Hz, 90/240 VAC Input Operation***

PHOENIX INTERNATIONAL

For our entire line of storage products: www.phenxint.com • Info: 800-203-4800
An ISO 9001:2000 Certified Service Disabled Veteran Owned Small Business

We Put the State of the Art to Work℠

Technology Focus

Thermal, Shock and Vibe Capabilities Drive Flat Panel Display Choice

As they shrink in size and drop in power consumption, flat panel displays are now ready for a variety of military vehicle and hand-carried systems. Choosing the right display involves careful consideration of vibration and management issues.

Tom Behnke, Product Manager, Displays
Computer Dynamics, a GE Fanuc company

Flat panel display systems offer many advantages for military applications. The technologies used in flat panel displays have advanced by leaps and bounds over the past several years. Innovations in panel physics have yielded better response times, better temperature ranges and longer life. LED backlighting technologies offer advantages over their CCFL (cold cathode fluorescent lamp) predecessors with regard to power draw, MTBF and brightness control. Board design or selection must take into account environmental conditions as well.

When integrating a board into a flat panel system, it is important to select a board that meets temperature requirements—keeping in mind that there will be a temperature rise inside the enclosure—and shock and vibration requirements, as well as other environmental conditions such as moisture. When LCDs and boards are properly packaged for the expected environment and are tested to military specifications, they become an optimal platform for visualization.

Active Matrix TFT LCD technology has made great strides in the past several years. Fueled by growth in the consumer market, research on flat panels has enabled manufacturers to make the images more vivid, have better black (i.e. block more light from the backlight), and have faster response times.

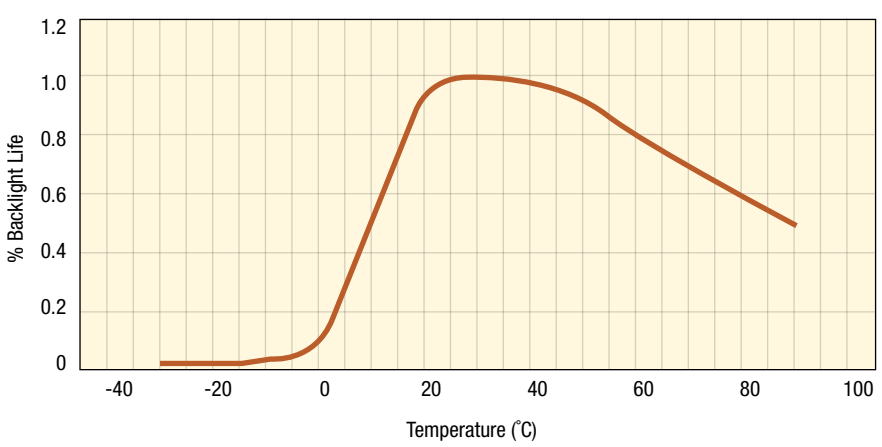


Figure 1

The weak link in TFTs is the CCFL bulbs that light the display. The penalty for turning on CCFL bulbs at low temperatures is severe. Plotted in this graph are the effects of temperature on CCFL life expectancy.

In all but the most extreme set of conditions, industrial grade LCDs will fit the bill for most military applications. In addition to better visualization benefits, many industrial grade LCDs offer better temperature ranges than their predecessors. It was once common to see LCDs offering an operational temperature range of 0-50°C. Many LCDs now offer ranges such as -20° to 60°C and better. It must be taken into account that most LCD manufacturers are giving an operational temperature range where all of the visualization characteristics given in the panel data sheet hold true.

If the user is willing to make some sacrifices with respect to brightness, response time and contrast, the panel can usually be safely operated slightly outside the operational temperatures given in a datasheet.

Two Hard Stops

There are two hard stops when it comes to operational temperature on LCDs. For common AMTFTs (Active Matrix Thin Film Transistors), at -40°C the liquid medium trapped between the layers of LCD glass freezes and could potentially crack the glass that holds it. Obviously this is not recoverable and must be prevented. On the upper temperature side, once the surface temperature of an LCD reaches its clearing temperature, the image on the LCD will fade to black. This is typically recoverable if the LCD is allowed to cool down to below this clearing temperature.

Another factor that affects LCDs is high ambient light. If an LCD is going to be exposed to high ambient light—and direct sunlight in particular—two negative effects can occur. First, there will be issues with glare and reflections. There are various films, coatings and treatments that will help negate the effects of high ambient light and further enhance the readability of the LCD. Second, when sunlight is an issue, solar loading effects become additive to the heat problem discussed above. To help reduce reflections, flat panel system manufacturers employ anti-glare coatings to the front of the panel. The coating works like a diffuser, changing the normal glass-like surface on the front of an LCD to a matte surface that stops reflections by scattering the light that bounces off the front of the LCD. To improve the contrast ratio and visual clarity of the LCD, anti-reflective films are usually applied on all transparent surfaces that interface with air to increase light transmission.

From a temperature standpoint, the weak link in TFTs is the CCFL bulbs that light the display. There is a severe penalty for turning on CCFL bulbs at low temperatures (Figure 1). This problem can either be handled from a system design standpoint with targeted heating at the bulbs or by using LED backlights. LED backlights are currently considerably more expensive than CCFLs, but prices are rapidly declining. LEDs bring many advantages to flat panel systems: wider operational temperature ranges, better dimming and lower power consumption to name a few.

Figure 2

An example of an integrated display solution is Computer Dynamics' Balefire. The Balefire is a sunlight-readable, military-grade monitor employing ruggedization technologies and methods to withstand the punishment of outdoor environments.

At the System Level

The LCD gets a lot of focus in a flat panel system design. After all, it is the component that users will be looking at, and it is typically the weakest component from a rugged environmental standpoint. Once the desired panel size, resolution and environmental and visual characteristics are determined and the desired panel is decided upon, it must be integrated into the flat panel system design. The flat panel system will be comprised of the flat panel display, a touchscreen (if needed), various boards and the enclosure for the system. Boards can run the gamut from complete SBCs to display modules—to convert various input video signals to a signal level suitable for the flat panel—to various support boards (inverters, temperature control boards and so on).

At the system level, special care must be taken in the integration of the flat panel display (Figure 2). At this point, shock and vibration as well as sealing become the major design considerations, and there are various methods for solving these challenges. The front surface of a TFT display is basically a thin sheet of glass. To protect this glass, there are several potential solutions including the use of a clear protective sheet (acrylic, for example) in front of the display that could also be used as a touchscreen surface if the application requires one.

Of course, adding a layer in front of the display can reduce the brightness from the backlights. To counteract this, anti-reflective films can be used at the air gap between the display and protective surface or the display and the protective surface can be optically bonded, eliminating the air gap altogether. There are various touchscreen technologies to choose from, each with their own benefits and drawbacks. Special care should

be taken to select the right technology for the current application.

Now that the display and possibly the touchscreen are selected, the various boards required for the application need to be determined. Depending on the backlighting technology used (CCFL or LED), a driver board must be selected. In the case of CCFLs, an inverter is necessary to create a high AC voltage to spark the fluorescent lamps. LED backlights require an LED driver board. If a touchscreen is used in the application, a touchscreen controller will also be necessary, which is typically a serial or USB connection back to the host PC.

Video Signal Formats

Industrial LCD panels require a digital video signal that is usually in either a TTL or LVDS format. This digital format can either be generated by a single board computer in the same enclosure as the panel or it can be generated from a standard video source such as DVI, VGA, NTSC, RS-170, or a multitude of other video standards. When the video format is not in a format that the panel inherently recognizes, it must be converted using a separate board that resides close to the LCD panel.

Finally, all of the components must be packaged together to meet the needs of the environment. Mechanical analysis needs to be performed to understand how to mount the LCD panels, boards, and possibly hard drives to meet the shock and vibration needs of the application. Additional mechanical analysis must be done to evaluate how temperature rise will affect the components in the system given the potential temperature extremes in the application.

Heating and cooling systems may need to be employed to keep component temperatures within their specification limits. Careful selection of materials used for construction of the system also needs to occur. Attention must be paid to materials that may be prohibited for use in the application, and materials should be used that will not promote fungus or mildew growth—if the equipment could potentially be deployed in a region where that is a concern). Systems must be designed to meet weight requirements and may require special heat-sinking as well.

Once the system is completed, it must run through a battery of tests to prove that the design will meet the application requirements. Various third-party testing facilities exist if a calibrated lab is not available on site. GE Fanuc Intelligent Platforms offers a variety of in-house testing capabilities including shock and vibration, emissions testing and temperature/humidity chambers (Figure 3). Any equipment used for testing should be calibrated at regular intervals and should be traceable by serial number for future reference. Test plans must be written and agreed upon by all parties involved so that an adequate testing process takes place.

Now that the design is proven through an adequate qualification process, the flat panel systems manufacturer must be

Figure 3

Once a display-based system is completed, it must run through a battery of tests to prove that the design will meet the application requirements. GE Fanuc Intelligent Platforms offers a variety of in-house testing capabilities like this on-site Temperature/Humidity Test Chamber.

able to reproduce multiple systems over the life of the program making sure that no changes occur that could potentially invalidate the system configuration as it was tested and qualified. The system manufacturer must have good processes in place that not only fully document how to build the system, but are also forward looking in their lifecycle management process to ensure that if an obsolescence issue with a component arises it will not jeopardize deliverables. From the standpoint of product lifecycle management, options include purchasing components to last the entire lifetime of the program or, if this is not possible, employing a method for regression testing new component integration to prove the design qualification is not affected.

Ready for Rugged Duty

The small size and decreasing power consumption of flat panels have moved display use from ships and control centers out into the battlefield where flat panel systems are installed in a variety of vehicles and can also be hand-carried. Of course, mobile applications bring other challenges into equipment design with regard to vibration and sealing.

By designing systems to meet those requirements, other challenges with regard to thermal management arise. Flat panel systems must balance the design to meet many system requirements and must be able to pass all required tests. Once the final configuration is established, the build must be controlled throughout its lifecycle making sure that no component changes occur without the proper analysis—even down to the passive component level. ▮▮

Computer Dynamics,
a GE Fanuc company
Greenville, SC.
(864) 627-8800.
[www.cdynamics.com].

Products

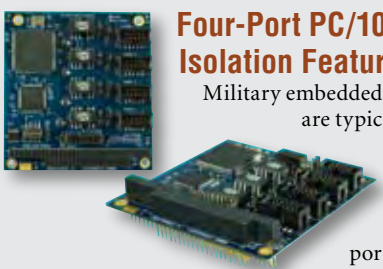
Get Connected with companies and products featured in this section.
www.cotsjournalonline.com/getconnected

Relay Module Boasts USB Optically Isolated Input

A number of defense applications must contend with high common-mode external voltages. Isolation is required to guard electronics from transient voltage spikes and offers greater common-mode noise rejection in electronically noisy surroundings containing industrial machinery and inductive loads. Targeting just that problem, ACCES I/O Products announces the latest addition to its impressive line of USB/104 I/O modules—Model USB-IDIO-16. The unit features 16 individually optically isolated inputs and 16 fully protected solid state FET outputs capable of switching up to 2A each. The USB-IDIO-16 is fully compatible with both USB 1.1 and USB 2.0 ports and offers hotplug functionality for quick connect/disconnect whenever you need additional I/O on your USB port. The circuit isolation makes the module ideal for use in control and instrumentation applications where high-voltage protection is required.

The USB-IDIO-16 can be integrated into any PC/104, PCI-104, or PCI/104-Express stack by connecting it to a USB 2.0 port usually included on board with embedded CPU form factors such as EBX, EPIC and PC/104—especially important since many newer CPU chipsets do not support ISA and have plenty of USB ports. The USB-IDIO-16 is price at $329; the USB-IDIO-8 at $259.

ACCES I/O Products, San Diego, CA. (858) 550-9559. [www.accesio.com].

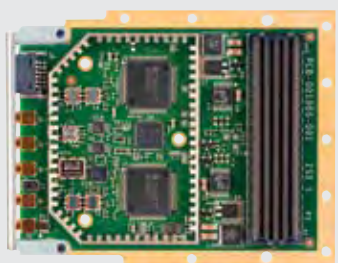


Four-Port PC/104 Serial Adapter Has Isolation Features

Military embedded systems that use PC/104 cards are typically deployed in remote locations where repairs are expensive and impractical. Sealevel Systems address that with its new optically isolated four-port PC/104 serial adapter. This new board, called the C4-104.485+I, has 1,500V DC port-to-port isolation and protects systems from ground loops and voltage transients that are common in remote installations and industrial environments.

For maximum versatility without opening the PC/104 stack, each port is software configurable for full-duplex (4-Wire) RS-422 or RS-485. Half duplex (2-Wire) RS-485 mode is also supported. The RS-485 enable signal is automatically controlled providing the highest level of data integrity and eliminating any risk of bus contention and data corruption. Jumpers on the board allow you to suppress ECHO on a per-port basis. The C4-104.485+I, part number 3547, is priced at $329 in low volume quantities. Standard operating temperature range is 0 to 70°C, and an extended temperature range version offering -40° to +85°C is also available.

Sealevel Systems, Liberty, SC. (864) 843-4343. [www.sealevel.com].



First FMC Rolls Out as Dual ADC Module

The FPGA Mezzanine Card spec, also called VITA 57.1, addresses the needs of FPGA-centric I/O by enabling I/O devices that reside on an industry standard mezzanine card to be attached to, and directly controlled by, FPGAs that reside on a baseboard. It's gaining interest quickly in DSP applications such as Signal Intelligence (SIGINT), Electronic Counter Measures (ECM) and Radar. VMETRO has rolled out the industry's first FPGA Mezzanine Card (FMC/VITA 57) module. The ADC510, available in air-cooled and conduction-cooled rugged versions, integrates two 12-bit 500 MHz A/D chips. This innovative design, based on the emerging VITA 57.1 standard, makes it easier for developers to integrate FPGAs into their embedded system designs.

The ADC510 supports two Texas Instruments ADS5463 ADC devices with each device supporting a sampling rate up to 500 Msamples/s and providing 12-bits of digital output. The ADC device interfaces are routed to the FMC connector to enable an FPGA on a baseboard to directly control and receive data. VMETRO makes available HDL example code for the ADC510 for integration into the HDL development suite for VMETRO FPGA baseboards.

VMETRO, Houston, TX. (281) 584-0728. [www.vmetro.com].

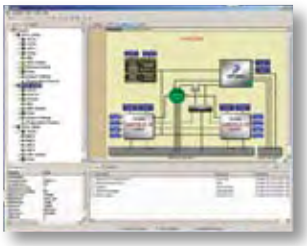
75W Tri-Output Converters Are Suited for Severe Environments

When design requirements call for operation in harsh environments, skimping on DC/DC converter choice is a bad move. Offering the right stuff for severe environment duties, Martek Power Abbott announces the release of the CB75T series, a 75-watt triple output device, expanding the choices available from the CB family of DC-to-DC power converters. Fully impregnated in a compact size of 2.0 x 2.75 x 0.5 inches, the highly reliable CB75T features a wide input range of 16 to 40 VDC and output voltages of 3.3 VDC or 5 VDC main, with ±12 VDC or ±15 VDC auxiliaries. Standard features include remote turn on / TTL, synchronization input, overvoltage protection, overcurrent protection and 500 KHz fixed frequency power conversion. Like all models in the family, the CB75T are available in I (unscreened) and M (screened) grades.

The design approach has maximized the power densities of the CB75T to over 27watt/in3, boosting efficiencies over 85 percent while maintaining a very competitive price. These together with full specified performance over an operating temperature range of -55° to +100°C from no load to full load make the CB75T ideal for mission-critical and severe environment applications. Pricing of the CB75T is $319 at 100 pieces (unscreened).

Martek Power Abbott, Torrance, CA. (310) 202-8820. [www.martekpowerabbott.com].

Get Connected with companies and products featured in this section.
www.cotsjournalonline.com/getconnected



Tool Suite Targets Multiprocessor System Apps

Developing software for military applications that scale over a few processors, or hundreds of processors is not easy task. Curtiss-Wright Controls Embedded Computing smoothes the way with the availability of Continuum Insights 2.1, an enhanced new version of its suite of GUI-based software tools for developers of embedded multicomputer systems application software.

The new version of Insights adds a powerful System Management tool to the Event Analysis tool and a System Monitoring tool previously included in the software suite. Continuum Insights improves the development environment for multicore SBC and DSP engine systems using Curtiss-Wright boards and Wind River Workbench, an Eclipse-based integrated tools suite. Continuum Insights expands upon the Wind River System Viewer tool for event analysis in multiprocessor systems, enabling the analysis of multiple multicore processors, both on a single board and across multiple boards. Continuum Insights 2.1 is supported on Curtiss-Wright's new VPX/VPX-REDI-based single board computers and DSP and FPGA engines, including the CHAMP-AV6, the VPX6-185 and CHAMP-FX2 products.

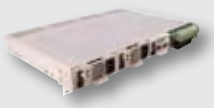
Curtiss-Wright Controls Embedded Computing, Leesburg, VA.
(703) 779-7800. [www.cwcembedded.com].

Three-Phase 600V IC Targets Motor Drives

Military systems are overflowing with motor subsystems performing a variety of tasks—from gun turret moving motors to aircraft wing motors. International Rectifier has introduced a rugged 600V three-phase gate driver IC for low, mid- and high-voltage motor drive applications including Permanent Magnet (PM) motor drives for micro inverter drives and electric vehicle drives. The IRS26310DJPbF integrates power MOSFET and IGBT gate drivers with three high-side and three low-side referenced output channels to provide 200 mA/350 mA drive current at up to 20V MOS gate drive capability operating up to 600V.

An advanced input filter is also integrated to reject noise and reduce distortion to improve system performance. The device's output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high-frequency applications. Available in 44-pin PLCC, pricing for the IRS26310D begins at $2.32 each in quantities of 100,000 units. Production quantities are available immediately.

International Rectifier, El Segundo, CA. (310) 726-8512. [www.irf.com].



Compact 1U Power Center Delivers 1,000 Watts

The increasing role of computing and communication gear used by the military is upping the ante when it comes to powering that gear. Feeding that appetite, TDI Power has introduced their ultra-compact 1U Power Center providing reliable -54V power, rated up to 1,000W all within one rack unit. Two hot-pluggable 500W rectifiers convert 90-276V AC into DC, which is distributed through up to ten GMT fuses. A connection to an external battery has an optional circuit breaker and Low Voltage Disconnect for optimizing safety and performance. The power center is monitored and controlled with TDI's eLink75 Ethernet controller.

Designed for use with remote, outdoor cabinets, the 1U Power Center helps manage site performance by providing power and signals for flush fans, door alarms and other environmental controls. For additional network awareness, an auxiliary 12V DC output can be used to operate an Ethernet switch with battery backup. Additional features include N +1 Redundancy, battery breaker and LVD and ruggedized assemblies with full conformal coating.

TDI Power, Hackettstown, NJ.
(908) 850-5088. [www.tdipower.com].

Military PDA Is Designed for Rugged Roles

Today's battlefield depends more and more on small information devices of various kinds. But they have to offer a level of ruggedness not found in consumer products. Along just such lines, Industrial Computing has introduced the Guardian 37 Military Personal Digital Assistant. The Guardian Military PDA is designed to provide a full range of computing functions in a PDA that meets Military specifications for shock, vibration and electromagnetic interference. These include MIL-STD-801F, MIL-STD-461E and MIL-STD-464A. Built to take a five foot drop onto concrete, waterproof and sealed, the Windows Mobile 6.0/Windows CE 5.0-based system can be adapted to a wide range of applications.

The 3.7-inch transflective screen with resistive touch screen is available in VGA and QVGA models and a full range of I/O capabilities are available. These include USB, RS232, RJ-45, CF, Stereo, Microphone and DC power. Communications capabilities include Bluetooth, WLAN, GPS and GSM/GPRS/3G/3.5G. The powerful battery allows a full eight hours of usage before requiring recharging.

Industrial Computing, Waltham, MA. (781) 890-3111. [www.industcomputing.com].

AC/DC Power Modules Enable Redundant Operation

Reliability ranks high when it comes to designing power subsystems for military applications. With that in mind, Lambda has extended its PFE series of AC/DC full-brick power modules with the introduction of the PFE500F that has additional features including active current-share and remote on/off. Like the existing PFE300S, PFE500S and PFE700S models, the new PFE500F versions provide a convenient AC/DC board-mounted solution with an output power of up to 504W for military applications.

The active current-share feature enables up to six PFE500F modules to be paralleled together to accommodate increased power requirements and/or redundancy. In addition, the positive logic remote on/off control and inverter-operation-good (IOG) functions provide greater flexibility in the start-up or shutdown sequencing and diagnostics of the power system. The fully regulated PFE500F models are available in 12V, 28V and 48V nominal outputs and can be adjusted over a ±20 percent range. The 12V PFE500F delivers up to 504W with a maximum base-plate temperature of 85°C, while the 28V and 48V models deliver the same output at temperatures up to 100°C. Line and load regulation is 0.4 percent and the efficiency exceeds 83 percent in all versions. The PFE500F series are available now with prices starting at $228 each in 100 piece quantities.

Lambda, San Diego, CA. (619) 575-4400. [www.lambdapower.com].

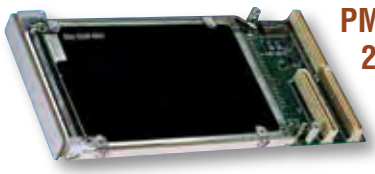
10-Watt DC/DC Converters Feature Compact Size

Today's brave new world of mix-voltage systems is driving demand for more power conversion, and the smaller the converters the better. Along those lines, Calex has announced the availability of the Calex 10-Watt EW Series. The 10 are housed in a 1.25 x 0.8 x 0.4-inch five-sided shielded case. The EW Series offers both single and dual output models. The input voltage ranges available are 9 to 18V, 18 to 36V and 36 to 75V. Single output voltages range from 2.5 to 15V and dual output voltages available are +/-5, +/-12 and +/-15 volts. All models are isolated input to output.

The switching frequency of the EW Series is 400 kHz. Efficiencies run as high as 87 percent typical. The input to output isolation voltage is 1500 volts DC. Output noise is only 50 mV peak to peak. Line and load regulation is 0.3 and 0.5 percent respectively. Output voltage accuracy is 0.6 percent. The operating case temperature range of the EW Series is -40° to +90°C.

Calex, Concord, CA. (925) 687-4411. [www.calex.com].

PMC SATA Drive Boasts 250 Gbytes of Rugged Storage

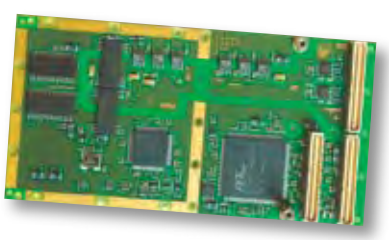


The transition to serial interconnects has touched every cranny of military embedded computing. In the storage realm that means the emergence of SATA. ACT/Technico has announced its SATA PMCDisk that replaces hard drives and disk modules that require external fixtures or system slots. For applications requiring moderate data storage, the SATA PMCDisk eliminates the need for SCSI-based storage while offering improved data transfer rates. The module can be used as a boot device as well.

Available with either rotating or solid-state flash SATA drives, the SATA PMCDisk can be used on any CompactPCI, VMEbus or VXS single board computer or carrier with a standard PMC slot, making the module ideal for a wide variety of commercial embedded systems in such industries as telecom, medical and industrial. Extended temperature versions are also available for more rugged environments, such as airborne and rugged ground applications. The SATA PMCDisk provides embedded system designers with cost-effective, flexible storage options. The 2.5-inch hard disk comes in storage sizes from 40 Gbytes to 250 Gbytes and the 2.5-inch flash drive is available up to 128 Gbytes. Pricing for a SATA PMCDisk starts at $800 with rotating storage.

ACT/Technico, Warminster, PA.
(215) 956-1200. [www.acttechnico.com].

Conduction-Cooled PMC Sports Dual Isolated CAN Links



The CAN bus, already entrenched in the automotive realm, is fast gaining mindshare in military vehicle designs. TEWS Technologies has announced the TPMC310, a conduction-cooled PMC (PCI Mezzanine Card) CAN solution that provides two complete CAN bus interfaces using Philips SJA100 CAN controllers. The TPMC310 is ruggedized for harsh environmental conditions. The CAN bus I/O interface provides two independent channels, isolated from system logic and from each other. Each channel supports CAN specification 2.0B and has the capability to transmit, receive and perform message filtering on extended and standard messages.

CAN High Speed transceivers are used for the CAN bus I/O interface. The I/O line configuration is configured by onboard solder pads for maximum reliability in a high-vibration environment. In addition, the TPMC310 meets the requirements to operate in temperature range from -40° to +85°C. Basic CAN software drivers available for VxWorks, LynxOS, LiNUX, QNX and Windows. In order to support long -erm programs, all TEWS' modules have a 5-year warranty.

TEWS Technologies, Halstenbek, Germany. +49 (0)4101 4058-35. [www.tews.com].

STRENGTHEN YOUR [ARM DESIGN EXPERTISE]

ARM® 2008 Developers' Conference

>Take advantage of the only design conference dedicated to a single architecture - ARM. Communicate, Connect and Create together with the largest partner community in the industry.

Here it is, under one roof! The ARM Developers' Conference is a unique showcase for ARM Partners across the development chain from SoC, embedded, Physical IP and EDA solutions to MCUs and application processors; from hot new software applications to the latest tools, methodologies, and OS developments. Nowhere else can you learn about the latest ARM processors, its road map and strategies, and how to integrate these into your next design?

drive your business [**FORWARD**]

A full 3-days of priceless information and contacts you can't afford to miss if you're currently designing or evaluating an ARM Processor-based application!

REGISTER NOW
for this Premium Event at the Santa Clara Convention Center, CA OCTOBER 7th-9th 2008

> Brought To You By:

ARM® ConVergence PROMOTIONS the RTC Group

www.arm.com/developersconference

Ultra-Compact Rugged Computer Serves up 100 GFLOPS

The stand-alone rugged box trend is becoming a major wave in the military design world. With its latest in that game, Mercury Computer Systems has released its PowerBlock 50 system, a high-performance, ultra-compact embedded computer designed for maximum performance in a minimal footprint, for small platforms in the 6- to 10-pound range. Optimized for real-time image, sensor and signal processing, and ruggedized for harsh environments, it is fully integrated and programmable, with state-of-the-art liquid cooling.

The system's modular architecture allows for flexible configurations of multiple processors, delivering well over 100 GFLOPS of processing power in a small, lightweight package. A fully configured PowerBlock 50 weighs less than 10 pounds, measuring approximately 4 x 5 x 6 inches—and can be held comfortably in one hand. The system is available now as the PowerBlock 50 EDK (Engineering Development Kit), which is a complete software development platform. Pricing for PowerBlock 50 EDK (Engineering Development Kit) starts at around $60,000. The EDK includes a PowerBlock 50 system, Linux-based board support package (BSP) development environment, cross-compile and debug tools, and a desktop heat rejection unit (HRU) to support cooling requirements. Complete systems are shipping today.

Mercury Computer Systems, Chelmsford, MA. (978) 967-1401. [www.mc.com].

Rugged Data Recorder Accommodates Diverse Drive Types

There's a growing need for data recorder subsystems that can withstand rugged or less than optimal conditions, yet provide high performance consistently and reliably. Designed to meet those rigorous demands, Conduant has announced the introduction of its Big River LTX2-35 data recorder. The new recorder is ruggedized for remote or portable applications and accommodates 3.5-inch hard drives, sealed drives or solid-state drives for greater flexibility.

The Big River LTX2-35 provides more than 500 Mbytes/s (4 Gbits/s) recording and playback performance in a space, weight and power efficient package. It can operate as a stand-alone system with network control or can be directly connected to a host computer via its StarFabric PCI bridge interface.

The 2U (3.5-inch) high chassis accepts 16 3.5-inch disk drives, for up to 16 Terabytes of storage capacity. The user may choose lower-cost, high-performance rotating disk storage or solid-state drives for more environmental tolerance such as shock, vibration, temperature, humidity and atmospheric pressure, depending on the application. Base pricing for the Big River LTX2-35 starts at around $34,000 for a 4 Tbyte system. Solid-state options are also available.

Conduant, Longmont, CO. (303) 485-2721. [www.conduant.com].

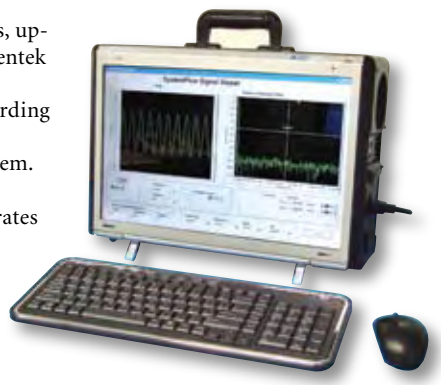
Smart Network Interface Module Has Three Channel IEPE

Digital communications is no longer the exception in military comms, it's the rule. Providing gear to support that trend, the Model 6006 from Vip Sensors is a 3-channel IEPE interface module with a fully digital communication interface incorporates all electronics for analog signal conditioning, analog-to-digital conversion, digital signal processing and RS-485 network communications. The gain and offset, filter corner frequencies and sample rates for the accelerometer are all programmable.

The Smart Network is a multi-drop transducer communication bus with a high data throughput that supports high-frequency measurements and a high level of synchronization for all channels connected to the network. A smart network controller card and PC software are used to communicate with all module channels connected to the network, for sending commands to each module, and receiving and storing sensor data. Vip Sensors offers a range of smart network sensors products and accessories in addition to the standard piezoelectric and voltage mode accelerometers, signal conditioners and cable assemblies. Shock and vibration calibration services are also available for all types of accelerometers.

Vip Sensors, San Clemente, CA.
(949) 429-3558. [www.Vipsensors.com].

Portable Signal Record/Playback Tool Streams at 500 Mbytes/s



A lot of military communications and radar applications require acquisition, down-conversion, analysis, up-conversion and reproduction of baseband and intermediate frequency (IF) signals. Feeding those needs, Pentek has announced its Model RTS 2721 Portable Signal Recording and Playback Instrument. Weighing only 23 pounds and measuring just 16.8 inches wide, 5.7 inches deep and 11.5 inches high, the product boasts recording and playback rates up to 500 Mbytes/s.

Packed into the RTS 2721 enclosure are 13 2.5-inch hard drives, one of which handles the operating system. The other 12 drives are configured as dual RAID arrays, dedicated exclusively for real-time recording and playback functions. This architecture guarantees no loss of data for sustained operation at the maximum rates and delivers a total storage capacity of 2.4 Terabytes. For example, this capacity supports continuous, real-time recording of a single 100 MHz A/D channel for three hours and 20 minutes. The price of the Model RTS 2721 Portable Signal Recording and Playback Instrument, including the Model 4990 SystemFlow Instrument Software, carrying bag, keyboard and mouse, is typically $59,995 depending on options.

Pentek, Upper Saddle River, NJ. (201) 818-5900. [www.pentek.com].

Product Development Based on Dedication, Innovation & Experience

Define the Requirements

- Understand Customer's Needs
- Product Specifications are Detailed
- Delivery Requirements are Identified
- Program and Product Costs are Defined
- Fixed-Price Proposals are Submitted

Engineering and Design

- Define the Range of Expertise Required
- Assign the Team Members
- Hardware, Firmware, Mechanical and Architectural
- Design Review Points to Ensure Compliance
- Designed for Testability

Production Phase

- Prototypes for Design Validation
- Pre-production Units for Manufacturability Validation
- Full Production Capability
- Customer Supply Chain Integration

Production Support Phase

- Product Life Cycle Plan
- Production Design Warranty
- Production Unit Warranties
- Long-Term Program Support Activities

Product Development

CDI's system engineering process transforms your requirements into a set of deliverables and process descriptions.

- Component Specification
- Product Development
- Systems Design
- Fabrication
- Test and Qualification
- Pilot Production and Production

Concept Development, Inc.

1881 Langley Ave
Irvine, California 92614-5623 USA
949.623.8000 P
949.623.8055 F

www.cdvinc.com

Celebrating 35 Years

Get Connected with companies and products featured in this section.
www.cotsjournalonline.com/getconnected

Fibre Channel over Ethernet Adapter Boasts Hardware Offload

As a back-end interface to networked storage, Fibre Channel holds a firm grip for data-intensive military systems. Mellanox provides an integrated single chip solution that delivers Fibre Channel over lossless Ethernet (FCoE) functionality and can reduce the number of adapters, cables and switches while improving the total bandwidth available with the potential to consolidate all of the traffic types over the same Ethernet link. The ConnectX dual-port 10GbE "converged" NIC from Mellanox includes support for both TCP/IP stateless offload and Fibre Channel transport in hardware.

The FCoE hardware offload includes processing of all CPU-intensive FC and SCSI processing tasks as currently available in high-performance FC HBAs, avoiding per-packet processing in software. This improves performance across the entire fabric (Ethernet and Fibre Channel) delivering significantly higher IOPs, throughput with better CPU utilization and reduced latency for networking, storage and clustering applications. ConnectX EN dual-port FCoE adapters, with support for PCI Express 2.0, are available today with various media interconnect support including XFP, SFP+, CX4 and 10GBaseT.

Mellanox Technologies, Santa Clara, CA. (408) 970-3400. [www.mellanox.com].

Mobile CAN Interface Links to USB

CAN and USB have both earned a warm welcome in military systems. IXXAT offers a low-cost single channel USB-to-CAN compact and dual channel USB-to-CAN II interface, which include a layer-2 Linux driver free of charge. This interface enables the development and the usage of customer-specific analysis, configuration and test applications on notebooks and other mobile systems. Due to the common driver interface, an adaptation of existing Linux applications to support the USB interfaces can be made very easily.

The Linux driver provides all functions necessary for the initialization of the CAN interfaces as well as for the transmission and reception of CAN messages. The easily configurable filter functions and message queues reduce the implementation effort considerably. The driver is delivered as source code and can be used flexibly by customer applications or adapted to specific customer needs. Besides Linux, IXXAT supports its interfaces e.g. with drivers for Microsoft Windows and VxWorks.

IXXAT, Bedford, NH. (603) 471-0800. [www.ixaat.com].

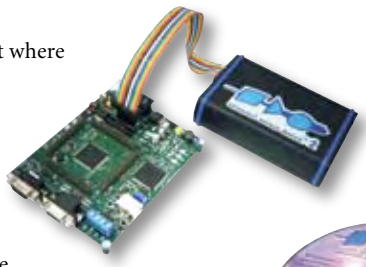
Real-Time Java VM Supports VxWorks

The Java language offers advantages in portability, scalability and modularity. PERC Pico from Aonix is a virtual machine for real-time Java and is now available for use with Wind River's VxWorks RTOS and Wind River Workbench development suite. The joint offerings provide developers with the resources to design complex mission- and safety-critical software within large teams where modular design is essential.

The PERC Pico development environment is geared toward the creation of resource-constrained and deeply embedded hard real-time applications and components and is based on the emerging Java Specification Request (JSR-302) for development of hard real-time safety-critical code. PERC Pico allows Java developers to write low-level Java code such as device drivers and interrupt handlers, telecommunications control plane, and signal processing for multimedia. It offers a memory footprint measured in hundreds of Kbytes in comparison to the tens of Mbytes required for other Java solutions as well as boasting performance, latency and determinism comparable to C.

Aonix, San Diego, CA. (858) 824-0212. [www.aonix.com].

Tool Aims at Freescale Multicore Debugging



The trend toward multicore processors shows no sign of slowing. That's good thing for the military market where compute density is top priority. Feeding that need, PLS Development Tools offers a Universal Debug Engine (UDE) that supports Freescale's MPC5510 Power Architecture 32-bit microcontroller (MCU) family. The high-performance MCUs, with an operating frequency of up to 80 MHz, are—depending on the device type—provided with: one or two Power e200z cores, up to 1 Mbyte of flash with error correction coding (ECC) and up to 64 Kbytes of SRAM. Moreover, the MPC5510 family of devices—designed specifically for use in body electronics—provide extensive communication interfaces (FlexRay, MultiCAN, LIN), DMA, low-power mode and additional typical peripheral units such as timer, analog-digital converter, and so on.

The connection to dual-core devices, such as the MPC5516, typically takes place via a single JTAG interface. In combination with PLS' Universal Access Device 2+ (UAD2+), download rates of up to 1 Mbyte/s can be achieved with the UDE 2.4. This guarantees users of the MPC5510 family a fast flash programming and also a short turnaround time during development.

PLS Development Tools, San Jose, CA. (408) 451-8408. [www.pls-mc.com/].

Small Module Blends Atom CPU and Rich I/O

Even the smallest, lowest power computer modules fall flat if they lack the necessary I/O functionality to succeed. A winner along those lines is the Conga-CA from Congatec. The card is an extremely low power consuming COM Express module that features the brand new Intel Atom processor Z500 series and the Intel System Controller Hub US15W. The Conga-CA module is a 95 x95mm (3 ¾ x 3¾ inch)-sized COM Express module and has a typical power requirement of less than 5 watt. Combining this with ACPI 3.0 battery management, ultra mobile embedded applications are now possible.

On the I/O front, the Conga-CA supports up to two PCI Express Lanes, eight USB 2.0, two Serial ATA, one IDE Interface and Intel High Definition Audio. Two onboard SDIO sockets allow for flexible expansion. Additionally, it features PCI bus, multi master I²C bus, LPC bus, fan control and Gigabit Ethernet. The Conga-CA is available in two different CPU variants. The Conga-CA eco version is powered by the Intel Atom processor Z510 with 1.1 GHz and 400 MHz front side and memory bus. The single unit price based on the Intel Atom processor Z510 with 1.1 GHz is $320.

Congatec, Deggendorf, Germany.
+49 991-2700-0. [www.congatec.com].

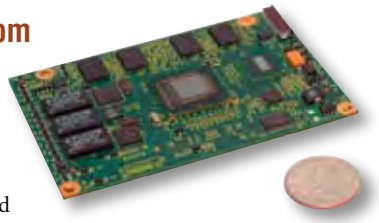
Boundary Scan Platform Enhances Mixed-Signal Test

The military embedded design world may be getting more digital all the time, but systems still need to talk to an analog world. That's why analog and mix-signal test is so critical. Geopel is keeping pace with a new JTAG/boundary scan I/O Module (SFX-Module) that features eight independent analog I/O channels with additional digital resources and supports application specific in-system reconfiguration. The SFX-6308 provides four output channels with extended current yield of up to 200mA at ± 10V and four bipolar input channels with a range of ± 10V. All channels have a 12-bit resolution and can be disconnected from the UUT via relays.

The module can be combined with any Scanflex controller (available for PCI, PCI Express, PXI, PXI Express, FireWire, USB and LAN). Standard features such as programmable range selection, external triggering and VarioCore technology make the SFX-6308 a versatile tool to test a variety of circuit functions, such as analog/digital converters, DC/DC transformers, digital/analog converters, digital potentiometers and extremely low-resistance input stages in interaction with boundary scan operations.

Goepel Electronic, Jena, Germany.
+49-3641-6896-739. [www.goepel.com].

COM Card with New Atom CPU Draws Under 5W



Fanless operation is a huge requirement in defense applications. The fan as a single-point of failure is too risky for most programs. Applied Data Systems has rolled out a new module that combines advanced power management with Intel's new Atom processor Z500 for a system-level power draw below 5W. The Catalyst Module is suited for low-power environments, so devices can be enclosed, without fans or heat sinks, while still supporting the latest multimedia, positioning and networking capabilities in portable, battery-operated, handheld devices.

The Computer-on-Module design of the Catalyst Module allows manufacturers to get to market quickly by separating the processor module from the I/O carrier card. Manufacturers have the flexibility to have Applied Data, other Eurotech member companies or a third-party create the carrier card to accompany the Catalyst Module. Applied Data offers a full-functioned carrier board in a Catalyst Module development system that manufacturers use to develop their application early in the process.

Applied Data Systems, Columbia, MD.
(800) 541-2003. [www.applieddata.net].

COM Express Card Suited for Battery-Powered Apps

COM Express has emerged as a popular form factor for non-backplane military systems. Adlink Technology's latest offering is a low-power COM Express type 2-compatible design based on the Intel Atom processor Z500 series with the new IntelSystem Controller Hub (SCH) US15W. Called the Express-MLC, this COM Express module is a highly integrated off-the-shelf building block based on PCI Express bus architecture that plugs into custom-made, application-specific carrier boards.

Although much smaller, Intel's Atom processor shares the same architecture as the new Intel Core 2 Duo processors and additionally supports Hyper-Threading Technology, a feature earlier introduced with the Intel Pentium 4 processor, allowing more than one code thread to be executed simultaneously on a single core processor. The Express-MLC will be available in a "basic" version that simply supports the feature set Intel Atom processor with the new Intel System Controller Hub US15W. The basic version supports two PCI Express x1, LVDS, SDVO, 8x USB2.0, SDIO, Audio and LPC-bus. The same module is also available with as an "extended" feature set and offers in addition to the basic features: PCI-bus, PCIe-based GbE LAN and PCIe-based SATA.

Adlink Technology, Irvine, CA.
(949) 727-2099. [www.adlinktech.com].

DISPLAYS GALLERY

Featuring the latest in Display technology

COTS Power Solutions for Military and Avionics Applications

- Introducing Calex CBAM™ Modules (Calex Brick Assembly Modules)
- Power Quality Modules MIL-STD 1275B Protects downstream circuitry against transients
- Filter Modules - MIL-STD 461E Filter for Conducted emissions
- Hold-up Modules Prevents power drop-outs during brownouts, transients, etc.
- Load Share Modules Easy paralleling of multiple converters

Calex Mfg. Co. Inc
Phone: (800) 542-3355
Fax: (925) 687-4411
E-mail: sales@calex.com
Web: www.calex.com

MIL-STD CUSTOM AND SEMI-CUSTOM SOLUTIONS

- Ruggedized for MIL-STD Use
- AC to DC and DC to DC Configurations
- Overcurrent and Overvoltage Protection
- Configurable MIL-STD Connectors
- Ethernet and RS232 Communications
- Conduction and Forced Air Cooling
- DC to DC with 96% Efficiency
- IP65 and IP68 Enclosures

ETA-USA
Phone: (408) 778-2793
Fax: (408) 779-2753
E-mail: sales@eta-usa.com
Web: www.eta-usa.com

5U Rackmount Dual 10" High-Bright LCD

- Dual High Bright 10" LCDs
- Extreme Temp Range
- 19" and 24" Rackmountable
- 461E, 810, 167, and Touchscreen Options
- Multiple Video Input Options
- U.S.A. Made: Designed, Engineered and Manufacturer in California

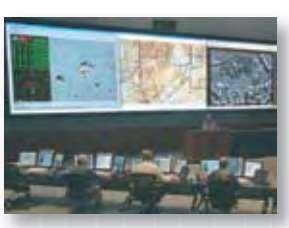
Neuro Logic Systems, Inc.
Phone: (805) 389-5435
Fax: (805) 389-5436
E-mail: Sales@NLSdisplays.com
Web: www.NLSdisplays.com/cots

2U Rackmount Dual 19" LCD and Sealed Keyboard/ Trackball

- Developed and sold to US Military
- Top/Bottom build uses less room when deployed
- Less "head-turning" allows for longer use by user
- 461E, 810, 167 Options
- U.S.A. Made: Designed, Engineered and Manufacturer in California

Neuro Logic Systems, Inc.
Phone: (805) 389-5435
Fax: (805) 389-5436
E-mail: Sales@NLSdisplays.com
Web: www.NLSdisplays.com/cots

Digitally Record & Stream High Resolution Imagery



- For virtually lossless recording or streaming, the DGy™ offers the state-of-the-art solution
- Caputre imagery at up to 2k x 2k pixel resolution
- Encode with advanced JPEG 2000 wavelet compression
- Record at 30 fps to local disks or net-work attached storage
- Stream to remote locations over LANS or WANS
- Playback with random access and event marks

RGB Spectrum
Phone: (510) 814-7000
Fax: (510) 814-7026
E-mail: sales@rgb.com
Web: www.rgb.com

ENH084SL3-550 8.4" SVGA AMLCD

- Enhanced performance for outdoor viewability
- Sunlight-readable, night-vision compatible
- 35% Increase over typical stock luminance
- SVGA 800(H) x 600(V) resolution
- 550 nit typical luminance
- LVDS Interface
- 6-Bit / 8-Bit selectable input signals
- Active viewing area: 170.4mm (H) x 127.8mm (V)

White Electronic Designs
Phone: (503) 690-2460
Fax: (503) 690-2490
E-mail: info@whiteedc.com
Web: www.whiteedc.com

Advertisers Index

Get Connected with technology and companies providing solutions now

Get Connected is a new resource for further exploration into products, technologies and companies. Whether your goal is to research the latest datasheet from a company, speak directly with an Application Engineer, or jump to a company's technical page, the goal of Get Connected is to put you in touch with the right resource. Whichever level of service you require for whatever type of technology, Get Connected will help you connect with the companies and products you are searching for.

www.cotsjournalonline.com/getconnected

COTS Journal (ISSN#1526-4653) is published monthly at 905 Calle Amanecer, Suite 250, San Clemente, CA 92673. Periodicals Class postage paid at San Clemente and additional mailing offices. POSTMASTER: Send address changes to COTS Journal, 905 Calle Amanecer, Ste. 250, San Clemente, CA 92673.

Coming Next Month

COTS JOURNAL

- *Vetronics in Manned and Unmanned Vehicles.* Onboard communications and control electronics (vetronics) are expected to multiply in sophistication for both next-generation and Current Force fighting vehicles. All that is putting pressure on system designers to find ways to meet the trickier cooling, shock and vibration problems that emerge when more computing gear is packed into those vehicles. This section looks at those developments as well as the technologies and solutions critical for vetronics. Included will be an update on the Army's Future Combat Systems program and Current Force upgrades that interrelate with that program.
- *Analysis: RoHS Two Years Later.* The commercial electronics industry embraced the European Union's RoHS initiative and never had to look back. But for the defense industry it's not so simple. The military market may be exempt from the restriction of hazardous substances (RoHS) initiative, but that doesn't mean makers of board-level products, for example, are off the hook. Most embedded computer companies craft board designs targeted for both military and non-military markets. Even companies purely in the military market can't escape RoHS's effects, because for some categories of components, lead-free versions are the only game in town. This section examines the test and analysis issues that complicate military system design in this era of RoHS.
- *Java vs. Ada for Defense Apps.* The military has good reasons for wanting to migrate toward Java. Using Java means leveraging the software industry's best tools and programming talent. Efforts are moving forward to solidify specs for real-time and safety-critical Java. Meanwhile, the Ada language offers unique features and an installed base that remains formidable. This section offers articles that track the latest on Java products and specification efforts, along with some comparisons between Java and the robust Ada 2005 language.
- *VME, VXS and VPX SBCs.* VME has earned an enduring role as the most popular embedded computer form factor for defense applications. Next-generation, fabric-based flavors of VME are coming together in the form of specs such as VXS (VITA 41) and VPX (VITA 46). This section updates readers on the progress of those implementations and displays a sampling of the current crop of VME, VXS and VPX single board computer (SBC) products.

portabledesign conference & exhibition

Power Management for a Wireless World

Conference sessions, Analyst Presentations and Panel Discussions on designing and powering portable, low-power wireless consumer devices.

- Complimentary Registration
- Keynotes
- Panel Discussions
- Technical Seminars
- Exhibition
- Lunch
- Networking Reception

September 18, 2008

San Jose, California

Wyndham Hotel

Attend for free. Register now.

www.portabledesignconference.com

an RTC Group Publication

PORTABLE DESIGN™

the engineer's resource for portable applications

sponsored by

mirasol™ QUALCOMM DISPLAYS

Actel®

expresslogic

tensilica®

COTS

Editorial

Jeff Child, Editor-in-Chief

Defense Industry, Meet Six Sigma

I've talked before in this column about the DoD's repeated attempts at reforming acquisition policy over the years. It's hard not to be cynical when round after round of lofty panel and committee discussions on Defense Acquisition Policy reform occur—starting as far back as 1986 and the David Packard commission. Despite those efforts, the problems don't seem to get solved. The vast majority of major weapon systems that are under development continue to miss costs, schedule and requirements goals. And the trend hasn't been improving. Costs and development time spans of major programs continue to increase.

All that said, my skepticism is beginning to fade a little as I look at the efforts Deputy Secretary of Defense Gordon England (see photo) has made to make some real progress in this area. I've been a fan of England since he took the reigns as Deputy SecDef in 2005. I like the fact that he comes from the industry, including a number of top executive posts at General Dynamics. Moreover, he, like myself, is a former electronics engineer, so he's got inside knowledge of technology and what makes the defense industry tick.

In his first year as Deputy SecDef, England set up a group called the Defense Acquisition Performance Assessment (DAPA) committee. Over the course of that year the panel analyzed all the aspect of acquisition—everything from requirements and organization, to decision methodology and oversight. Fortunately, transcripts of most of the DAPA committees' meetings were made public. And I remember being impressed by how many of the panel's insights and themes of discussion rang true with things *COTS Journal* readers deal with, such as process improvement and hardware/software integration.

One of the points back then raised by DAPA panel member retired U.S. Army General Paul Kern, was the lack of policy advocating continuing process improvement. While corporations like General Electric focus on a Six Sigma process, and Toyota, a lean production process, the DoD always seems to be quick to craft regulations and policy and then call it correct, instead of continuously trying to improve it.

While many of the vaunted DoD reform efforts of the past had little follow up, the DAPA initiative did lead to some new real actions. The most recent of these came last month with Secretary England issuing a directive that all Defense Department components adopt Lean Six Sigma, a continuous improvement methodology derived from systems engineering and operations research.

Issued on May 15, the directive instructed all sections and segments—"components" to use their language—of the DoD to use Lean Six Sigma to improve productivity, mission performance, safety, flexibility and energy efficiency. The process-improvement methodology seeks to reduce variability and eliminate waste. In April of last year, England started that ball rolling by having the Office of the Deputy Undersecretary of Defense for Business Transformation put in place the new Continuous Process Improvement/Lean Six Sigma Program Office in order to expand the use of Lean Six Sigma throughout the DoD. The new directive signals the growing importance of Lean Six Sigma in the DoD's business transformation efforts. The directive instructs all components to retain the savings generated by CPI/LSS improvements and use them to further enhance their operational capabilities. It also asks all components to offer career development opportunities related to CPI/LSS, and include CPI/LSS in employee performance plans when appropriate.

Deputy Secretary of Defense Gordon England

Personally, I like the step the DoD is making to essentially institutionalize a kind of continuous process-improvement scheme. And by using Six Sigma, which is an established, proven practice used in a number of industries, there's some real basis now for measuring success. It appeals to my engineering background. Engineering focuses a lot on making things work and improving designs to make them work better.

That entails an iterative process, where success is achieved after iterations of prototypes and testing. Score one for Gordon England. Change can come slow in an entrenched industry like the defense industry, but kudos to England for pushing it in the right direction. With a presidential election on the horizon, there's no way to predict whether England or someone of his caliber will be in charge of acquisition policy next year. But either way, England has at least raised the chances of making progress there. ▮▮

High-Speed USB Solution to Data-Enable Tactical Radios

Warfighters can transmit/ receive GPS maps, images, coordinates, and IM communications.

- USB synchronous radio adapter cable
- High-speed data throughput
- Interoperable (Send/receive data with different radio models and brands)
- Hot swappable

Available with a variety of radio connection options that make it compatible with the most prevalent brands and models:

Harris PRC-117	Raytheon ARC-231
Harris PRC-150	Raytheon PSC-5D
Thales PRC-148	Motorola LST-5
Rockwell Collins ARC-210	

Call and ask about your specific models.

Sealevel Systems has the high-speed solution to data-enable tactical radios: a USB synchronous radio adapter cable and free DISA PDA-184 software. Connect the plug-and-play cable to your computer or handheld device via USB[1] and to your tactical radio. It's that quick and easy for warfighters to enhance their critical high-speed data communications in the battlefield.

The PDA-184 software is government-developed, government-owned by DISA and is available from Sealevel as part of this total solution.[2] Features include:

- Implements MIL-STD-188-184 Data Waveform
- Easy-to-use Java-based GUI
- Runs in Microsoft Windows XP or 2000

Contact us at **864.843.4343** or **sales@sealevel.com**

[1]Also available with PCMCIA connection.

[2]Able Communications Technology Corporation, under contract to DISA, provides engineering and software development expertise for the PDA-184 Software in addition to supporting the revision of MIL-STD-188-184 along with other UHF SATCOM MIL Standards.

Proud to be American owned.
Committed to American made.
Honored to have 20+ years serving the military.

SEALEVEL®
864.843.4343 | sealevel.com

POWER ON DISPLAY

Today's high performance rugged aerospace and defense applications demand previously unreachable levels of embedded processing and graphics display capabilities. For system integrators the design and packaging challenges loom large. Curtiss-Wright is a step ahead with their next generation of VPX single board computers and XMC graphics display/video capture solutions. The VPX6-185 SBC is a Power Architecture™ Single Board Computer delivering high bandwidth and performance along with Serial RapidIO™ and PCI Express® switched fabrics. The VPX6-185 with its PCI Express-based XMC mezzanine support is an ideal host for Curtiss-Wright's new XMC-710 graphics controller card powered by an NVIDIA® G73M graphics engine with dedicated video memory and Curtiss-Wright graphics IP. This combination provides unmatched graphics capability to solve complex applications with new levels of visual quality, integrity, and speed.

Curtiss-Wright's VPX6-185 VPX dual Freescale 8641-based single board computer and the XMC-710 dual output/input video XMC deliver leading, high bandwidth processing and graphics display performance. Together they provide integrators an ideal rugged embedded subsystem solution.

CURTISS WRIGHT Controls
Embedded Computing

Innovation In Motion.
cwcembedded.com

VPX PROCESSING AND XMC GRAPHICS... *ABOVE & BEYOND*